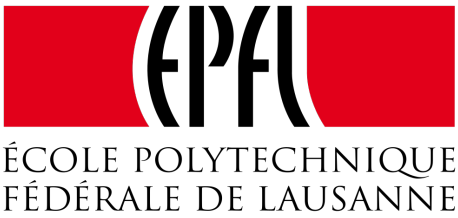


ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Institute of Microengineering

GR-LVT

Master Thesis

Development of a microfluidic interface for suspended microchannel resonators

Author
Damien Maillard

Supervisor
Annalisa De Pastina

Professor
Prof. Luis Guillermo Villanueva

Fall semester 2016-2017

January 20, 2017

Abstract

Suspended microchannel resonators (SMRs) are devices that detect particles in liquid samples. In comparison with similar resonating devices that must be immersed, SMRs allow the fluids to flow through microfluidic resonators. This principle of operation leads to a great reduction of the required sample volume and to enhanced quality factors. As such, SMRs show great potential for a variety of sensing applications.

This thesis reports on the final steps of the microfabrication of SMRs and on the development of a microfluidic interface allowing the assembly and operation of those devices. The interface connector was drawn in SolidWorks before being fabricated. Two different techniques were then used. 3D-printing allowed for rapid prototyping of the connector, and different versions were produced. The final device was machined out of PMMA by a mechanical workshop. Sealing techniques were studied for vacuum operation of the SMRs. After reviewing a few different methods, we adopted an o-ring-based solution. In a similar manner, we selected fluidic connections that best suited the interface.

Simulations were conducted to ensure the viability of our solution. In particular, the deformation of silicon nitride microchannel ceilings under o-ring compression was studied.

Few experiments were performed with a 3D-printed connector, assembled to a simple PMMA lid and to an actual SMRs chip previously fabricated. It allowed us to evaluate the performances of 3D-printed devices and gain important insights in the assembly and handling of the fluid delivery system. Although the PMMA connector was not tested, it is expected to work admirably, as it possesses numerous advantages over its 3D-printed counterpart.

Keywords : suspended microchannel resonators, biosensor, microfabrication, microfluidics, world-to-chip interface, packaging, vacuum sealing, o-ring sealing, 3D printing

Acknowledgements

I would like to express my profound gratitude to my supervisor, Annalisa De Pastina. Throughout my master project, she has been very supportive of my work and has always been available. Our discussions, along with the numerous pieces of advice she supplied on a daily basis, have been invaluable to me.

I would also like to thank Prof. Luis Guillermo Villanueva for offering me the opportunity to conduct this project in his lab. I have really appreciated his supervision and help during those last four months.

On a more general note, I am thankful to my colleagues from the ANEMS group for the great working atmosphere they provided.

I am also grateful towards the microsystems laboratories (LMIS) 1 and 4 for granting me access to their labs and allowing me to work and conduct experiments there. Without their equipment, I would not have been able to carry out this project as easily. In particular, special thanks go to Enrica Montinaro from LMIS1 for providing fluidic connectors samples, as well as to Matthieu Ruegg from the same lab for his help with the 3D printer. I am also thanking Guillaume Petitpierre and Ludovic Serex from LMIS4 for the time spent giving me trainings on the CO_2 laser and the *neMESYS* syringe pump, respectively.

I would like to thank Mr. Alfred Thomas, as well as the whole *ATPR* mechanical workshop, for the manufacture of our PMMA connector. The few meetings I had with Mr. Thomas regarding the design of our connector were very insightful.

Finally, thanks go to the CMi (Center of Micronanotechnology) for their help in the clean room for the fabrication of the devices.

Contents

List of Tables

List of Figures

1 Introduction

Suspended microchannel resonators (SMRs) are established sensing devices. Their ability to detect molecules without being immersed in the sample of interest gives them two main advantages over other resonator-based fluid sensing techniques : lower fluid samples and higher quality factors.

An important component of all microfluidic devices is the packaging. Developing a reliable and practical chip integration can save great amounts of time that are better dedicated to performing experiments.

This project is thus oriented on two very different aspects of microfluidic devices. On one hand, fabrication of SMRs devices needs to be finalized. In particular, the electrodes have to be deposited, trenches to reduce the parasitic capacitances need to be defined, and the resonators have to be released. On the other hand, a microfluidic integration has to be developed from scratch.

This thesis is organized as such : Section 2 starts by briefly reviewing the SMRs with a strong focus on the existing packaging solutions. Then, Section 3 reports on the different fabrication steps performed in the clean room and Section 4 lists the choices made in the design of the interface. Finally, Section 5 checks the viability of the solution with simulations and Section 6 explains the brief experiments conducted, along with their conclusions.

2 State of the art

In this work, we start by briefly reviewing the developments made with suspended microchannel resonators. After a quick overview, we mainly focus on the two domains of interest of this project : fabrication and packaging.

2.1 Overview of the device

The idea of using resonant channels for sensing was developed by Enoksson et al. [1]. They presented a device made of a silicon tube whose resonance frequency changed according to the density of fluid flowing through. The sensor consisted of a tube in a double-loop arrangement designed for torsional vibration (Figure 1).

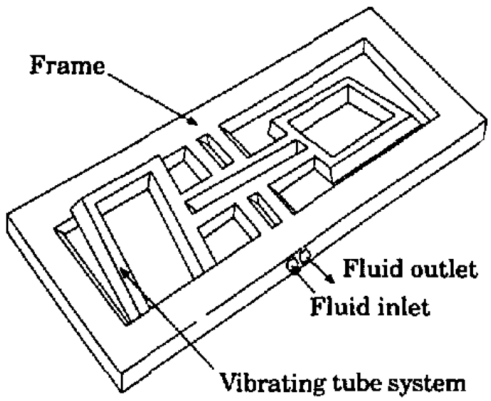


Figure 1: Device developed by Enoksson et al. for fluid sensing. Depending on the density of the fluid, the torsional vibration operated at different resonance frequencies [1].

In 2003, Burg and Manalis published a first paper about suspended microchannel resonators (SMRs) for biomolecular detection [2]. The device consisted of functionalized microfluidic channels embedded in a cantilever driven at resonance frequency (see Figure 2). A shift in the measurement of that resonance frequency was detectable as biomolecules accumulated on the channels walls or simply flowed through the device.
The biological samples targeted for detection are generally part of body fluids, such as blood or saliva for example. The main motivation behind the development of SMRs lied in the

deterioration of the mass sensitivity and frequency resolution arising from operating a resonant beam mass sensor in a liquid environment. Affected by damping and viscous drag, cantilever-based biosensors have shown quality factors decreasing by two orders of magnitude if they are being operated in water instead of air [3]. Enclosing the fluid inside the resonator itself allowed to drive the cantilever in a free environment without degradation of the quality factor when the fluid was run inside the microchannels. Additionally, the necessary sample volume was significantly reduced.

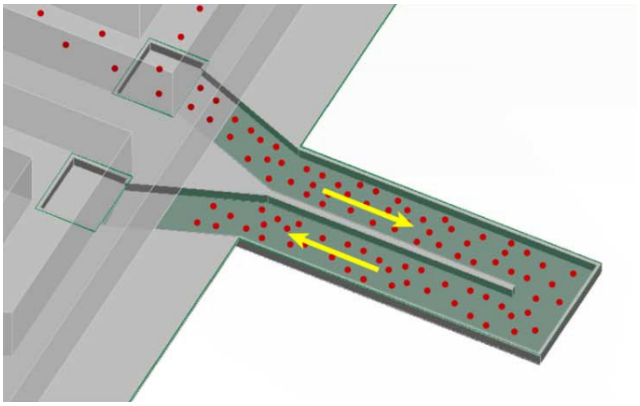


Figure 2: Schematics of a suspended microchannel resonator : the microfluidic channel is enclosed in the cantilever [4]

In 2006, Manalis' group published a solution to encapsulate and operate SMRs in vacuum. They showed that the quality factor of fluid-loaded beams was increased by more than six times in comparison with operation in air. Moreover, the frequency stability over a time scale of thirty minutes was significantly enhanced, allowing to characterize slow binding molecules or low concentrations [4].

More recently, SMRs performances have been continuously improved, and new applications have been developed, allowing for example to weigh single cells and nanoparticules [5].

2.2 Fabrication

In this section, we study different fabrication techniques used to realize suspended sensing devices.

Enoksson et al. fabricated their silicon resonant tubes using two 100 mm-diameter, 500 μm-thick, double-side polished (100) silicon wafers [1]. The interior of the sensors were defined by photolithography, using a 2 μm-thick silicon dioxide mask. The two interior halves of the tubes were etched in a KOH solution to a depth of 400 μm (leaving a bottom thickness of 100 μm).

The wafers were prepared for bonding by a treatment in a (2.5:1) mixture of H_2SO_4 and H_2O_2 at 110°C for 10 minutes, and then bonded in a mask aligner with a wafer-to-wafer pattern accuracy of 5 μm. Subsequently, the full bond strength was completed by heat-treatment in a 1150°C oxygen atmosphere for 1 hour.

New silicon dioxide masks were then defined on both sides of the wafer pair, to define the exterior of the tubes, similarly to the interior walls. Taking advantage of the anisotropic etching processes, the tube structure had six walls with a thickness of about 100 μm (see Figure 3).

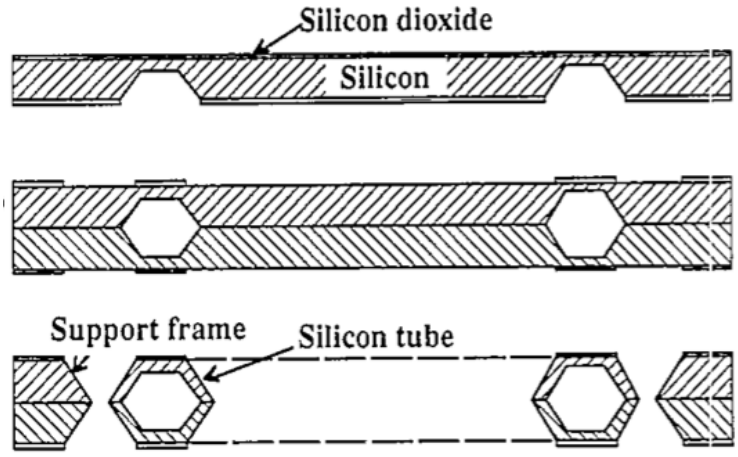


Figure 3: Brief process flow of the fabrication of Enoksson's resonant tubes [1].

To fabricate their first suspended microchannel resonators back in 2003, Burg et al. combined a polysilicon Damascene process, a sacrificial layer etching and bulk micromachining

[2].

At first, the channels were defined in a standard $\langle 100 \rangle$ silicon wafer with reactive ion etching. Then, the wafer was covered with 800 nm low-stress low-pressure silicon nitride (creating the bottom and the side walls of the channels) and 1.5 μm poly-silicon (sacrificial layer temporarily filling the channels). A chemical mechanical polishing (CMP), timed to stop when the silicon nitride layer was reached, followed. Afterwards, a second layer of low-stress silicon nitride with the same thickness as the first layer was deposited, closing the filled microfluidic channels. RIE was subsequently used to pattern the two joined silicon nitride layers to define the resonators, as well as access points to the channels. Simultaneously, the back-side was also patterned to define, under the devices, the location of the through-holes for the release. Finally, the wafer was put in a 6 M aqueous potassium hydroxide solution at 80°C to etch the poly-silicon inside the channels and release the devices.

In their publication of 2006, Burg et al. followed the same process flow up to the deposition of the second nitride layer. The main difference lied in the fact that the channels were emptied and released at different times. First, inlets were defined in the silicon nitride, allowing KOH to access the sacrificial poly-silicon. After emptying of the channels, a 50-nm layer of chromium was patterned on the resonators by ion beam deposition to provide high reflectivity (for optical detection) and serve as electrode (for electrostatic actuation). Subsequently, the silicon nitride layers were both etched to define the resonator outline and the sample delivery holes (on both sides of the wafer). The resonators were finally released in tetramethylammonium hydroxide (TMAH) [4].

2.3 Actuation and detection

SMRs have long been actuated electrostatically. The silicon tube sensor developed by Enoksson et al. was operated with an external electrode situated about 30 μm away from one of the corners of the tube loop [1]. To a similar extent, Burg et al. coated the suspended microchannels with layers of aluminum [2] or chromium [4].

Barton et al. used a different, photothermal-based actuation method [6]. A 405 nm amplitude-modulated diode laser was focused on the device and brought pulses thermal energy at a given frequency. The device layer undergoes subsequent thermal expansion and

contraction, setting the device into motion.

Detection was initially achieved with the optical lever method [2, 4, 5]. A laser beam was shone and reflected back by the top surface of the cantilever, with an angle depending on the bending of the cantilever. Collecting the reflected beam with a photo-detector, it was possible to determine the amplitude and the frequency of the device's flexural motion.
Lee et al. integrated piezoresistive sensors to characterize the motion of their SMRs [7]. Piezoresistors were implemented by doping the top silicon layer of the device via ion implantation. To enable detection, a Wheatstone bridge needed to be developed in parallel.
Very recently, a capacitive sensing method was published to detect the lateral motion of suspended nanochannel resonators [8]. Two electrodes were disposed on each side of the resonator. One of them was responsible for electrostatic actuation, and the second one was used to measure the capacitance variation between the resonator in motion and the electrode.

2.4 Packaging

In this section, we are reviewing microfluidic packaging solutions. For more clarity, we decided to separate this chapter into three parts focusing on different aspects of the "macro-to-micro" interface. In each subsection, a particular attention is given to solutions developed for SMR devices.

2.4.1 Vacuum sealing

Polydimethilsiloxane (PDMS) has long been the favoured material when it comes to seal microfluidic devices. In addition to being inexpensive and rather easy to process, it offers mechanical flexibility, optical transparency and biocompatibility, making it an evident choice for various applications [9]. Moreover, an extensive knowledge of its properties has been acquired, allowing to bond it to various materials. The important disadvantage of a PDMS sealing is its incompatibility with vacuum operation. Indeed, its high permeability to gas and liquids impedes maintaining a satisfactory level of vacuum at chip level [10]. The possibility of fluids diffusing between isolated channels through the PDMS cannot be rejected either.

The literature is packed with PDMS interfaces designed for microfluidic devices. In the scope of suspended microchannel resonators, Burg and Manalis used a microfluidic network made of PDMS bonded to the chip for their first devices and were thus restricted to make their experiments in air [2].

In 2000, Corman et al. presented a wafer level vacuum packaging for resonant fluid density sensors [11]. Here, we focus on a solution developed specifically for suspended microchannel resonators : in 2006, Manalis' group encapsulated their SMRs in a wafer-scale vacuum packaging made of glass [4]. Glass was chosen to ensure transparency for the subsequent detection via the optical lever method. The process flow is depicted in Figure 4.
Bonded to a glass wafer, a silicon wafer was etched in potassium hydroxide down to a layer thickness of 20 μm. The silicon was then patterned using deep-reactive ion etching (DRIE) to form a mask for the channel etch (Figure 4(a)). Subsequently, the glass was etched in hydrofluoric acid (Figure 4(b)) and the main parts of the silicon mask were removed by DRIE. Small islands were remaining on the side of the chips to act as hard spacers during the bonding process (Figure 4(c)). A gold film with adhesion layers was then deposited (Figure 4(d)) and patterned (Figure 4(e)) for the electrostatic actuation of the devices. Finally, glass frit was silk-screen printed onto the substrate (Figure 4(f)), and the glass wafer was bonded to the silicon wafer containing the devices under vacuum (Figure 4(g)). A drawback of this sealing method is that it does not permit the operation of the device in air conditions once the bonding is done.

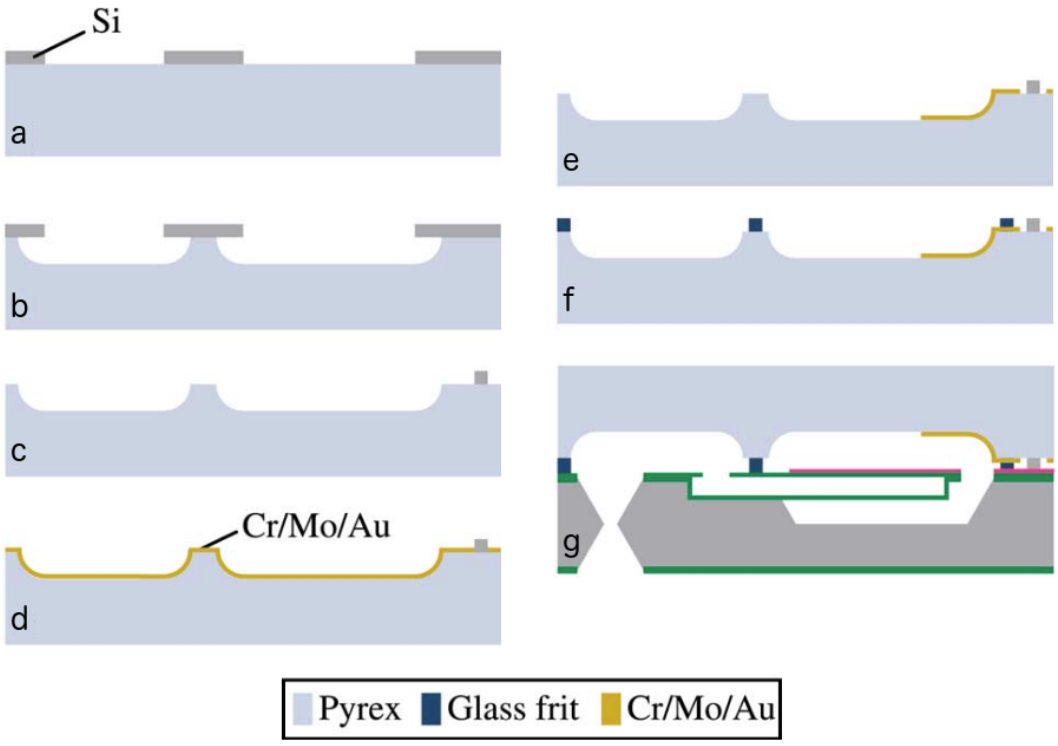


Figure 4: Process flow of the vacuum-packaged SMRs from Manalis' group [4].

In his doctoral thesis, Khan followed a modular approach featuring a completely reversible assembly of SMRs chips [12]. Similarly to Burg and Manalis, he brought the fluids from the bottom of the chip and could efficiently isolate the fluidic inlets from the vacuum chamber situated on top. Figure 5 depicts an exploded view of this packaging. A PEEK fixture was machined with a cavity to hold the chip. Directly on top of the chip, an o-ring was placed for vacuum sealing. This o-ring was compressed by an aluminum capping with four screws. The capping was made of a central vacuum chamber that would be connected to an external vacuum pump with an horizontal channel. On top of this aluminum element, a second vacuum o-ring was placed. The interface was finally completed by a glass slide to ensure hermeticity.

The two main advantages of Khan's packaging over Manalis' were reversibility and flexibility in the operation environment. First, this interface was economical as the assembly elements were reusable after quickly switching between chips. On the contrary, Manalis built a package for each chip, yielding considerable clean room costs. In addition to that, Khan's devices could be tested in air or in vacuum whether the vacuum pump was connected or not.

Ciftlik et al. developed a poly (methyl methacrylate) (PMMA) fluidic adapter [13]. To ensure sealing, an o-ring was again positioned between the chip and the PMMA element (Figure 6). While this solution was not intended to work in vacuum, the use of PMMA as sealing material was highly interesting for us.

The packaging solutions presented so far are not ideal for prototyping. Designing molds or masters for PDMS and machining fixtures or adapter elements are time-consuming and can lead to great expenses. Researchers have thus looked at new materials and rapid-prototyping techniques [9]. 3D printing has emerged as a fast and reliable method for the realisation of complex microfluidic interfaces. Here, focus was set on 3D printing with stereolithography, because this technique enables the realisation of transparent devices [14].
The stereolithography technique was patented by Chuck Hull in 1986 [15], and the first commercialised system arrived in 1988. It consists in building objects by successively curing layers of materials via ultra-violet light. Basically, a platform is soaked in a bath of curable resin. Photopolymerization of the resin is then performed by a scanning laser on

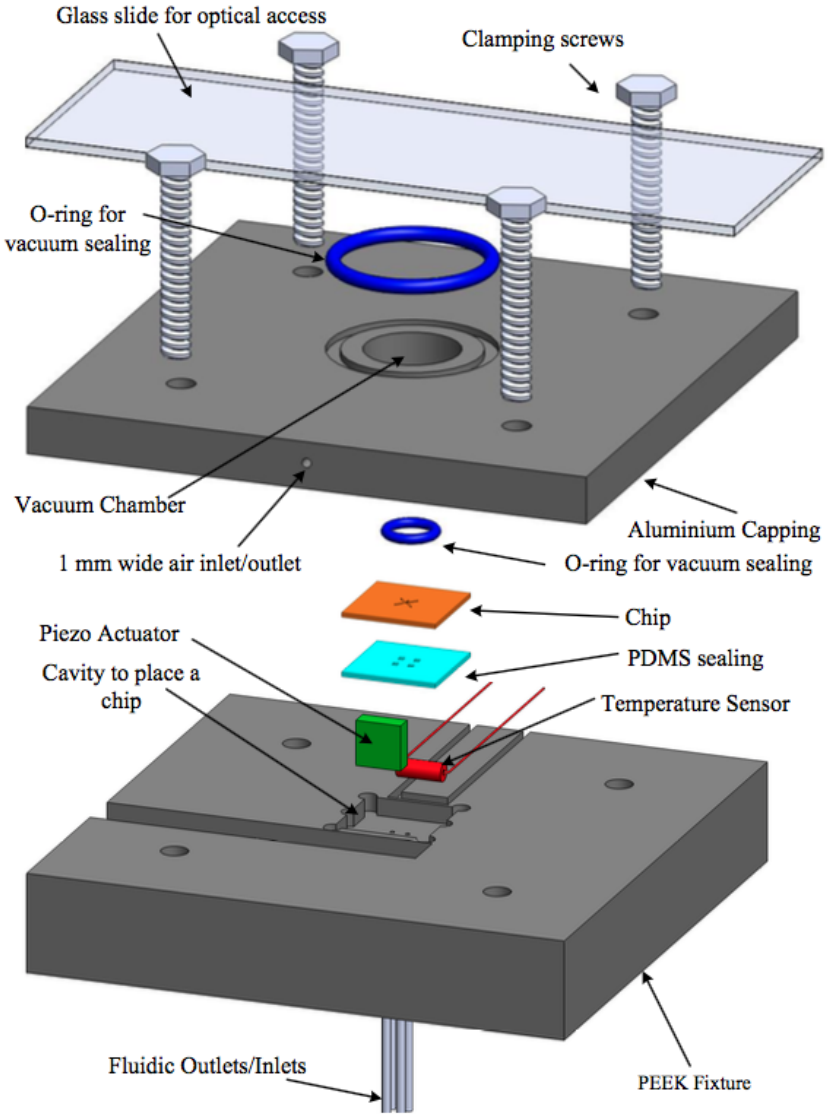


Figure 5: Khan's packaging solution to ensure vacuum operation of the devices [12].

planes parallel to the platform. After a layer is completed, the platform moves up or down depending on the system configuration (see Figure 7) [16].

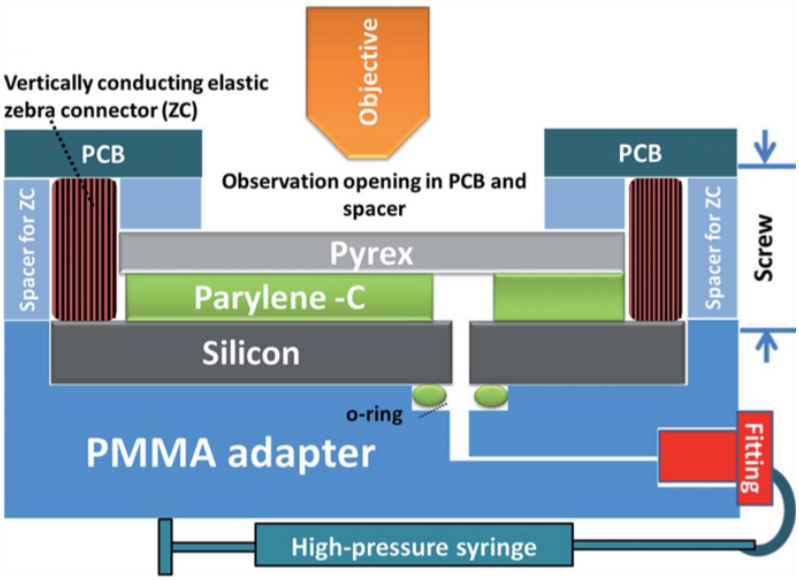


Figure 6: Schematics of a packaging solution involving a PMMA adapter [13].

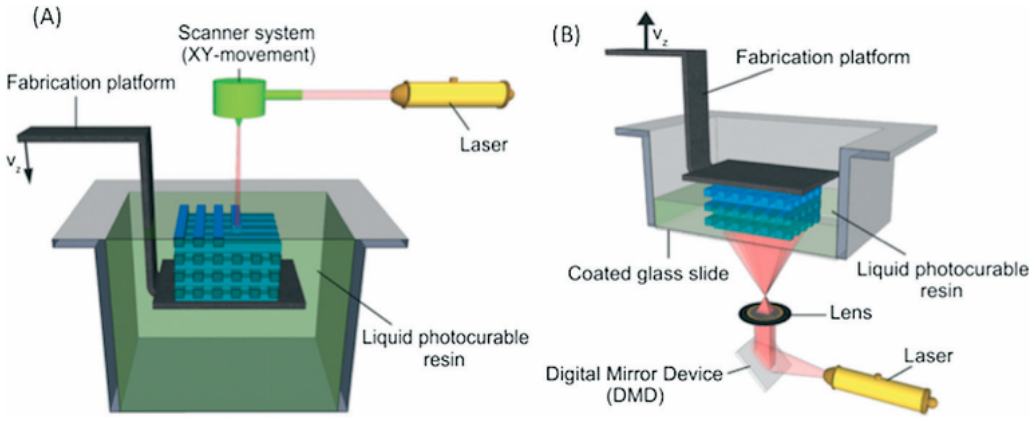


Figure 7: Schematics of two stereolithography configurations. (A) Bath configuration where the platform is moving down. The scanner system enables X and Y movements. (B) Bat configuration, where the platform is moving up. A Digital Mirror Device allows the laser light to expose the surface quicker [16].

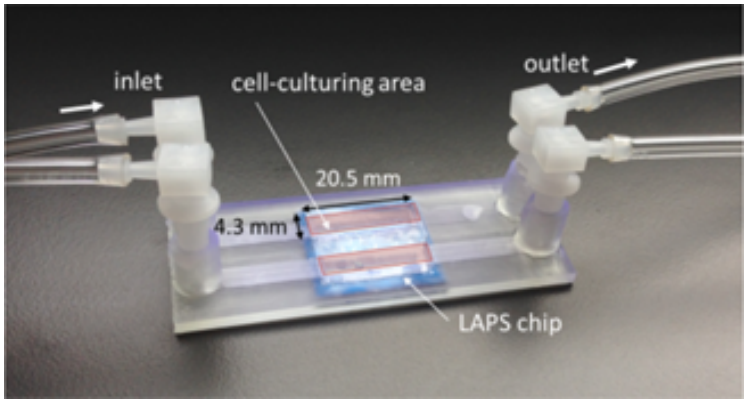


Figure 8: Microfluidic assembly developed by Takenaga et al. for encapsulating an LAPS chip [17].

Takenaga et al. used a 3D-printer (Asiga, PicoPlus 27) to create a microfluidic assembly for a light-addressable potentiometric sensor (LAPS) chip [17]. Figure 8 shows the complete interface including the inlets and outlets. The biocompatibility of the cured resin was studied by monitoring cell growth curves obtained from culturing them in the microfluidics-based LAPS. The results were similar to those achieved with cell culture flasks, indicating that the assembly was biocompatible.

2.4.2 Fluidic connections

As their importance is sometimes neglected, fluidic connections tend to be the least reliable component of microfluidic devices and often limit their performance [9]. In this subsection, we review numerous methods, with a particular emphasis on solutions developed for SMRs.

Temiz et al. highlighted the most important features of a good fluidic interconnect : minimal dead volume, no cross-contamination of samples, easy to plug, removable and reusable, low-cost and chemically inert, among others [9].

The importance gained by PDMS in microfluidic devices induced numerous developments in compatible connections. Inserted, reversible connections have been considered for many applications. As an example, press-fit connectors are a popular solution. Compatible with moderate pressures and easy to plug, those connections take advantage of the compression

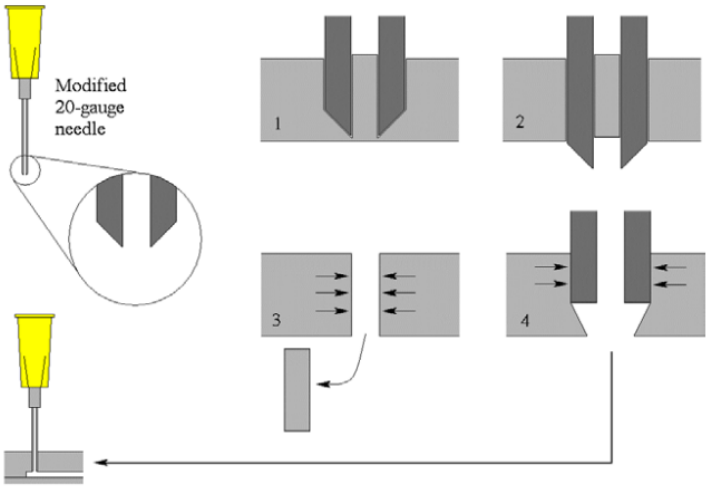


Figure 9: Schematics of press-fit connection fabrication method [18].

sealing between the PDMS and the inserted needle. As an example, we elaborate on the method studied by Christensen et al. [18]. A gauge needle first had its flat-tipped outer edge shaped to a sharp edge. This modified needle was then used to bore a cored hole with a diameter equal to the inner diameter of the needle. Removing the needle and inserting a new, unmodified needle created a compression seal, because the outer diameter was larger than the hole (Figure 9). On the other side, the needle was connected to a luer connector. it was found that those interconnects could be disassembled and remounted numerous times without importantly degrading the sealing quality.

Perozziello et al. used custom-made PDMS rings as a seal between a 3-layer PMMA chip and subsequently inserted metallic tubes [19]. The rings were fabricated from polycarbonate (PC) molds machined by micromilling technology. The intermediate PMMA layer was machined with cavity to house the rings, as well as through holes on the back-side for fluid transport. After insertion of the PDMS rings in their housing, the three layers of PMMA were thermally bonded together. Finally, the metallic tubes were inserted. Figure 10 shows molds used for fabricating the elastomeric rings, along with a complete assembled chip with fluidic connections.

The inserted methods reviewed did not require resistant custom-designed fixtures bearing the significant force ensuring leak-free connections. On the other side, their main drawback

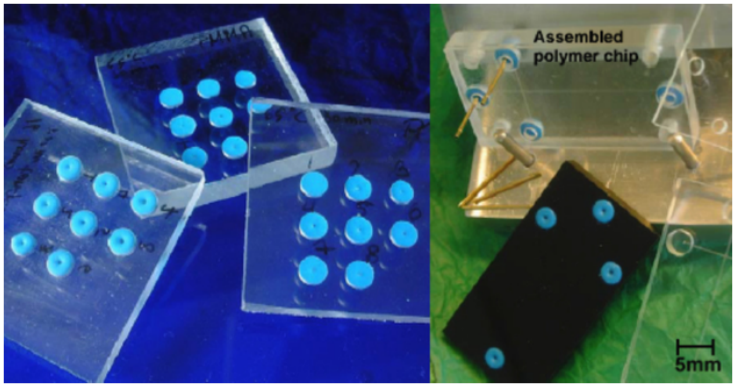


Figure 10: On the left, molds used for custom-made elastomeric rings. On the right, assembled PMMA chip with integrated fluidic interconnections. [19].

is that they restrict from integrating high-density connections [9].

Contact-based connections have therefore been developed. Those solutions consist of a soft intermediate element, such as a polymer gasket or an o-ring, and an adaptive part held in compression against the soft medium to ensure leak-free connection with the chip.

Snakenborg et al. took advantage of flexible tubings [20]. The tubes were inserted into a flat-bottom hole continued by a smaller diameter hole. Following, a thread was machined for connection to standard fittings. On the other side, the hole depth was such that the flexible tubing would exceed it and a small part would come out. Compressing a chip onto the tube, the latter was deformed laterally, squeezing the central opening and ensuring a leak-free connection (see Figure 11).

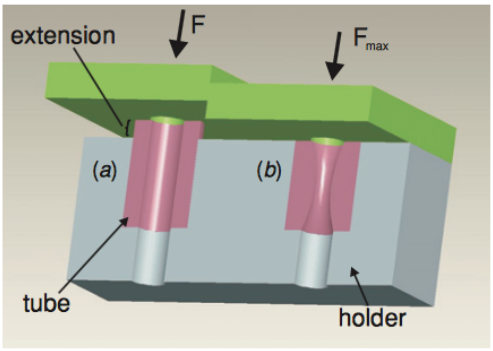


Figure 11: Cross-sectional schematics of a tube-sealing interconnection. On the left, before being compressed, the tube length exceeds the hole's depth. On the right, the sealing is achieved by compressing the tube into the hole, squeezing the central opening to ensure a leak-free connection [20].

Another contact-based technique, using o-rings, has been used in the specific application of SMRs. In their wafer-level vacuum packaging for SMRs, Burg and Manalis built a Teflon (PTFE) manifold holding standard 1/32" (0.794 mm) tubes [4]. The holes were drilled with smaller diameters, and the fixture was heated for insertion of the tubes. The chip, assembled to a PCB, was clamped in the manifold. Finally, the interface was completed by sealing the manifold against the chip's back surface with perfluoroelastomer o-rings and clamped. The sealing was ensured up to a pressure of 150 psi (10.34 bars). The complete interface, including the electrical interconnections, is depicted in Figure 12.
This solution offers reversibility in the fluidic connections. As the interface can be easily disassembled, the manifold can be cleaned or replaced easily.

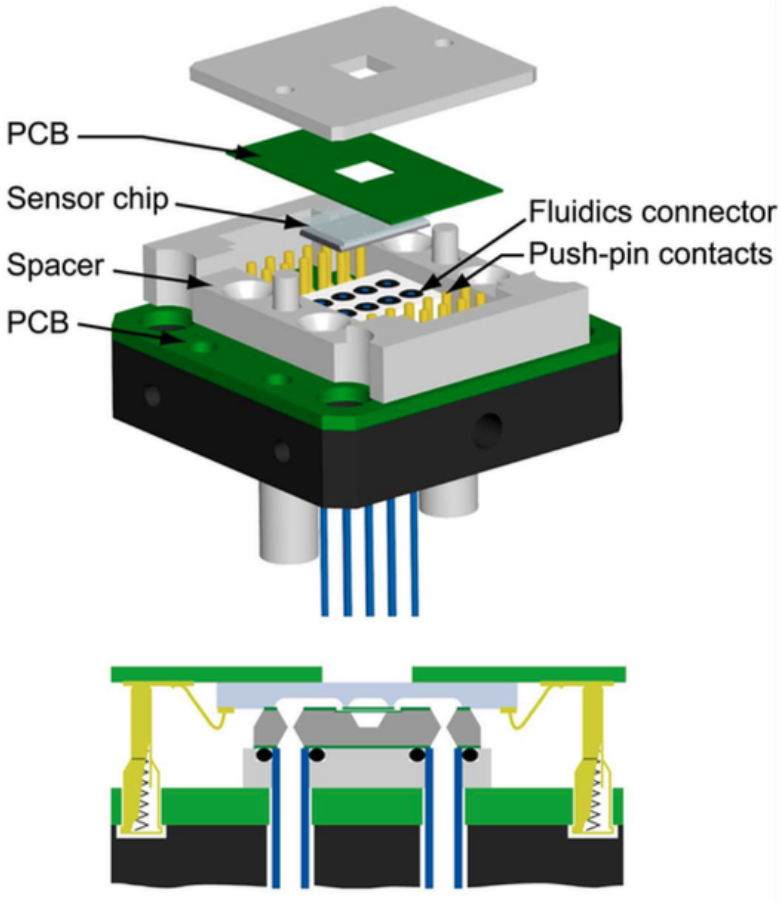


Figure 12: Packaging solution ensuring vacuum sealing developed by Manalis' group [4].

In his interface, Khan opted for a similar approach (see Figure 5). Four holes were bored through the PEEK fixture in alignment with the inlets of the chip. On the backside, larger holes, in which metallic tubes were subsequently hermetically inserted, were drilled. Inside the cavity, a PDMS seal patterned with a CO_2 laser was placed between the PEEK surface and the chip.

This subsection is concluded with the review of a simple irreversible connection. Permanent sealings are unique to each chip, inducing a great cost increase. On the other side, they are necessary if the application requires high pressures.
Glavan et al. used strong double-sided adhesive tapes to seal commercially available microfluidic ferrules to a paper-based microfluidic device ([21], Figure 13).

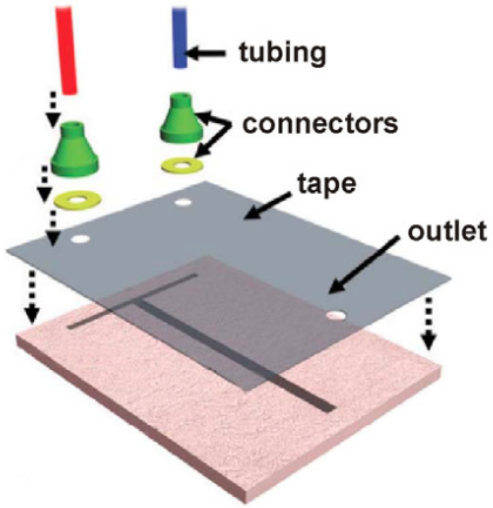


Figure 13: Packaging solution with an intermediate double-sided adhesive layer ensuring sealing between the chip and commercial microfluidic ferrules [21].

2.4.3 Electrical connections

The actuation and detection of the motion of suspended microchannel resonators can be achieved by different means (see Section 2.3). As the ultimate goal is to have an integrated and compact device, without external sources of actuation or detection, it is required to implement electrical connections. Those connections can be either reversible or permanent.

When the contact pads are located on only one side of the chip, edge connectors and sockets are convenient to use. They are easily and reliably pluggable with the mechanical alignment being achieved through the edges of the chip [9]. Those connectors can be world-wide standards, such as SD or microSD, or can be designed specifically for an application. An edge connector was for example used by Temiz et al. to connect cyclic voltammetry devices to external electronic circuits [9]. The contact pads were made of 20 platinum contacts (as seen in Figure 14). The main disadvantage of this type of connection is that it drastically reduces the flexibility of contact positioning. It is not possible to use such electrical interconnects if the pads are disposed on more than one side of the chip.

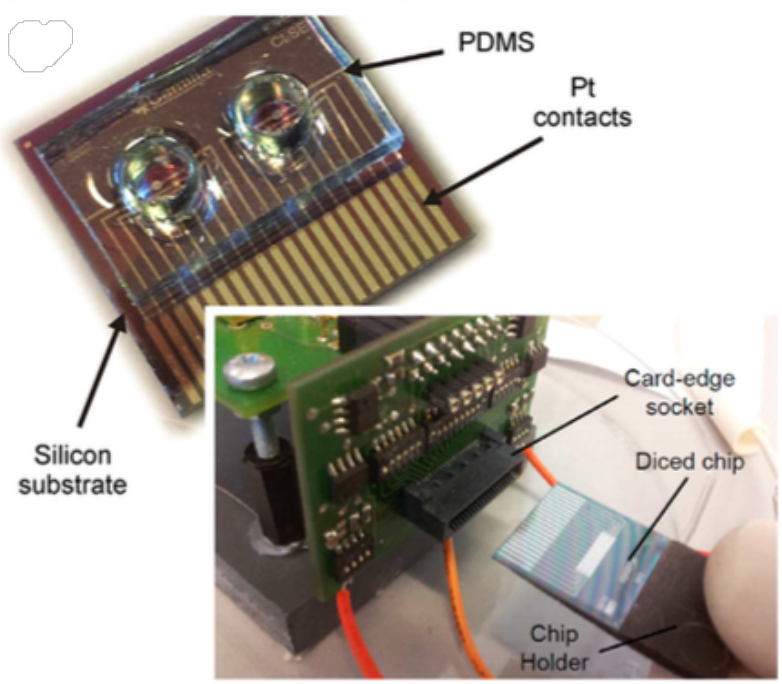


Figure 14: Edge connectors providing a reversible electrical connection for the driving electronics of cyclic voltammetric detection of analytes [9].

Spring-loaded contacts enable the arrangement of contact pads in any format. Those pins are generally mounted on a PCB or a platform and compressed to achieve contact. As an example, spring-loaded contacts were disposed on a Plexiglas ring by Park et al. [22]. An intermediary PDMS gasket was used between the chip and the Plexiglas ring (Figure 15).

Packaging fixation was achieved with screws at the center and on the periphery of the ring and ensured both electrical connection with spring-loaded contacts and fluidic sealing with SU8 microchannels.

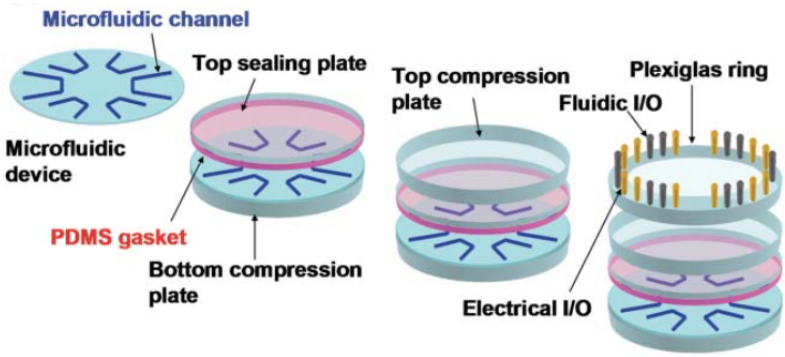


Figure 15: Schematics of an electrical connection achieved with spring-loaded contacts. The contacts are disposed on a Plexiglas ring compressed onto the chip with an intermediary PDMS gasket [22].

A great deal of applications use an intermediary PCB to electrically connect the chip to external circuitry. If the contact between the chip and the PCB pads needs to be permanent, wire-bonding then becomes the obvious choice.

In their vacuum-operated device, Burg and Manalis designed all pads for wire-bonding on the glass wafer [4]. To accomplish a stable electrostatic drive, it was further required to contact the metallized surface of the resonators. This was achieved with a silver filled epoxy connecting the chip's chromium to a metal trace on the glass. The chip, along with its capped glass wafer, was then attached to an adhesive back printed circuit board (PCB) and the electrical connections were completed via wire-bonding (see Figure 12). The assembly was further clamped into a manifold and the PCB pads were connected to another PCB via spring loaded contacts.

3 Microfabrication

In this work, we focused on the second part of the fabrication of suspended microchannel resonators in clean room. The process flow was entirely developed and optimized by Annalisa De Pastina. We are only reporting on the steps actually performed, i.e. starting at step 12 of the run-card (found in Appendix) and continuing until the devices are completed.

The last process previously conducted (at step 11) was a chemical vapour deposition of low-stress silicon nitride. Empty channels were located immediately under the silicon nitride layer. Since the channels are very fragile, particular care had to be observed from the beginning when handling the wafers.

3.1 Bottom contact

3.1.1 Sputtering

The bottom contact was deposited with the *Pfeiffer SPIDER 600*, a sputtering tool. The working principle is briefly described : first, a plasma (partially ionised gas containing an equal number of positive and negative charges) is generated. Then the ions are projected onto the target, and pulverise atoms. Those atoms diffuse towards the substrate and condensate at the surface, forming a thin film [23].

Before depositing the bottom contact on the top layer of silicon nitride, a procedure had to be followed. First, all targets needed to be cleaned. For each material of interest (Al, Pt and SiO_2), we loaded dummy wafers and ran a cleaning step. It basically consists in depositing target molecules for a few minutes. In addition to that, we monitored a test-sputtering of aluminum nitride. This process is particular. Indeed, the target is simply made of aluminum, and nitrogen is brought to the chamber during the process to mix with aluminum and deposit on the wafer. The parameter that is critical to check is the reflective power. If this power is too high, not all the forward power goes to the sputtering chamber, preventing a full control of the AlN deposition.

The deposition of the bottom contact consisted of 15 nm of aluminum nitride and 25 nm

Slot	ID	Task	Recipe	Step	T [°C]	Time	Thick.	Power [W]	sccm
25	dum.	SiO_2 clean	SiO2 clean target	1	RT	-	-	1000	-
23	dum.	AlN prep	AlN_prep_350	1	300	-	-	1500	-
21	dum.	Pt clean	Pt_T_clean_target_350	1	300	-	-	1000	-
23	dum.	RP check	AlN_T_D1	2	300	5:00	-	1500	40/10
19	7674	AlN-15nm	AlN_T_D-1_Pt_T_D_Etch_D1	3	300	0:19	15nm	1500	40/10
		Pt-25nm			300	0:06	25nm	1000	-
17	7672	AlN-15nm	AlN_T_D-1_Pt_T_D_Etch_D1	3	300	0:19	15nm	1500	40/10
		Pt-25nm			300	0:06	25nm	1000	-
19	7674	SiO_2-20nm	SiO2_F	4	RT	1:00	20nm	1000	-
17	7672	SiO_2-20nm	SiO2_F	4	RT	1:00	20nm	1000	-

Table 1: Parameters used for the deposition of the bottom contact.

of platinum. On top, 20 nm of silicon dioxide were sputtered as a protective layer for the subsequent photolithography. As photoresist could become challenging to remove, residues may stick to the wafer even after the strip. This sacrificial layer of oxide ensured that the platinum surface stayed clean. Moreover, when SiO_2 was subsequently etched in hydrofluoric acid, the potential residues sticking to the surface would be removed with the oxide.

Table 1 summarizes all the parameters used for the deposition, which was performed on two wafers (IDs 7672 and 7674).

After the process, we checked with a multimeter that the oxide was correctly deposited. Probing different locations on the wafer, and particularly the same electrode pads, the multimeter reached a maximum detectable resistance, labelled overload (O.L.). An overload result corresponds to a resistance in the hundreds of $M\Omega$ range, which we consider here equivalent to non-conduction. It was thus confirmed that the silicon dioxide completely covered the underlying platinum layer.

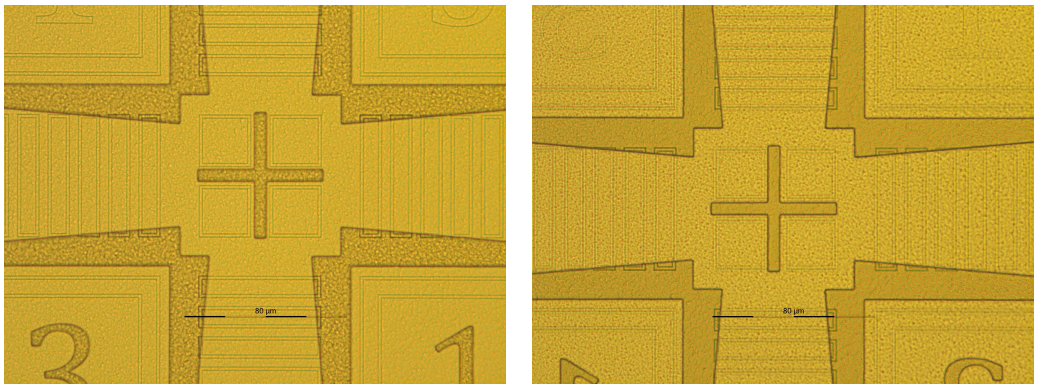
3.1.2 Photolithography

The photolithography of the bottom electrode features followed the deposition. Wafers 7672 and 7674 were coated with 2 μm of AZ ECI 3027 positive photoresist. We used the program 0326 in the *ACS200*, an advanced coater/developer tool. An HMDS treatment for promoting the adherence of the photoresist to the oxide, as well as an Edge Beam Removal (EBR) step to remove photoresist on the edge of the wafer, were included in the program.

The exposure was performed with the *Heidelberg MLA150 Photoresist LASER Writer*. The mask designs were converted with the high quality mode and the parameters of the exposure were a laser wavelength of 405 nm, a dose of 150 mJ/cm^2 and a defocus of -3.

The development was done in the *ACS200* with the corresponding program number : 0926.

Subsequently, we inspected our wafers at the *Optishot 200* optical microscope. Figure 16 depicts the successful cross alignments accomplished on wafer 7674. Wafer 7672 exhibited similar results.
Additionally, we had a deeper look at the photoresist features. The pattern of the bottom contact was defined in the photoresist and represented the features transferred to the underlying substrate, as described in Section 3.1.3. Figures 17 and 18a show photoresist on top of microchannels and the dimensions of the features measured for chips 2 and 15 of wafer 7674 respectively (Appendix describes the chip numbering). As a comparison, Figure 18b details the theoretical sizes of those same features as they were designed on CleWin. We notice that the photoresist covered completely the underlying microchannels on both wafers and that its width was adequate (25 μm). Nevertheless, we remark that the alignment turned out finer on chip 2 than on chip 15. On that last chip, even if the photoresist covered only approximately 1 μm more than the microchannel, it was still an acceptable result allowing us to continue with the etching.
The first alignment after the channels had been defined was challenging for different reasons. The markers on which we performed the cross alignments with the *MLA* were made of 1 μm trenches that were difficult to see. Moreover, the wafer was not completely flat. Indeed, numerous depositions had been achieved at high temperatures up to this point. For those reasons, the alignment was not uniform everywhere on the wafer.



(a) Left cross *(b) Right cross*

Figure 16: Successful alignment of the bottom contact mask on the first mask (3 to 1 alignment marks) on wafer 7674. Pictures taken with the Optishot 200 microscope, with a magnification of 50x.

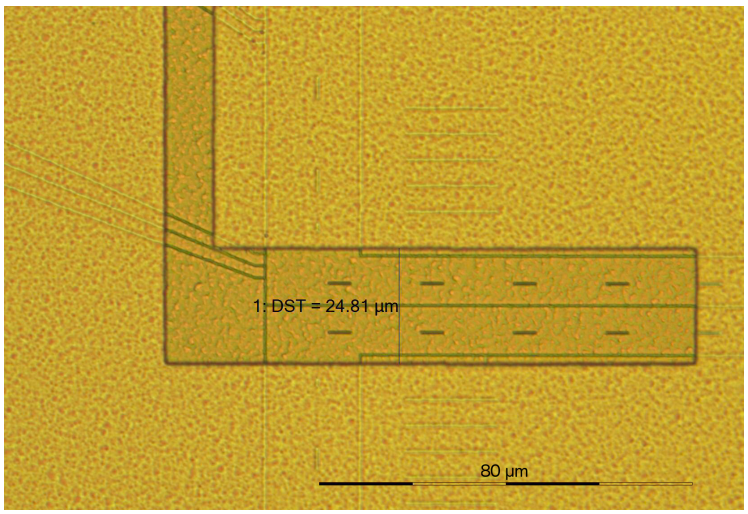
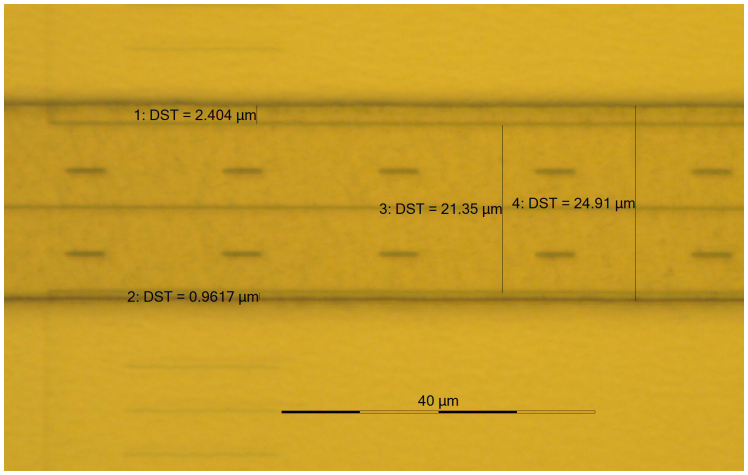
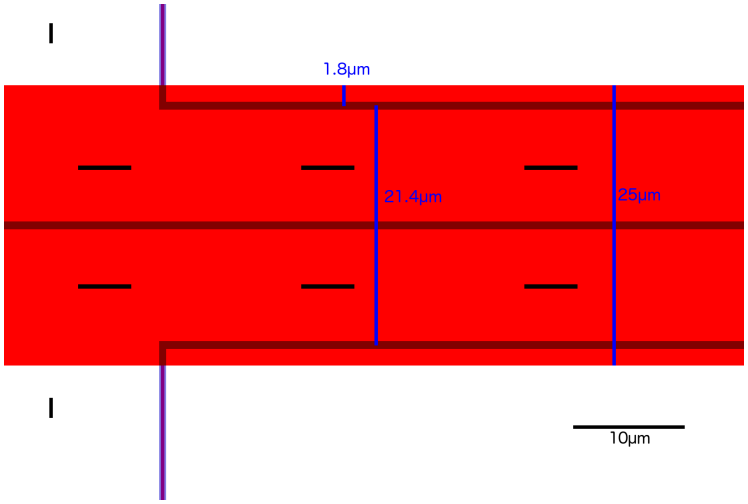


Figure 17: Bottom contact photoresist feature on chip 2 of wafer 7674. We notice that the width of the electrode is close to the design (25 μm, Figure 18b) and that the photoresist area is perfectly centered with respect to the underlying channels. Picture taken with the Optishot 200 microscope, with a magnification of 50x.



(a) Bottom contact photoresist feature on chip 15 of wafer 7674. The width of the feature is adequate, but the photoresist area is misaligned with respect to the channels. Picture taken with the Optishot 200 microscope with a magnification of 100x.



(b) Bottom contact features sizes as defined in CleWin.

Figure 18: Size of the features of bottom contact photoresist topping a cantilever as measured and in theory. Even if the photoresist was slightly misaligned, we could continue with the etching, because it was completely covering the channels.

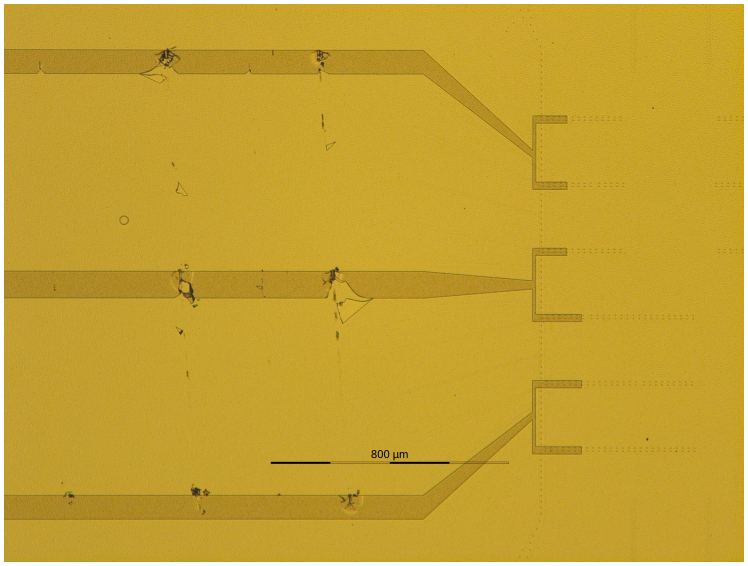


Figure 19: Bottom contact photoresist on the left side of chip 15 on wafer 7672. It appeared that the photoresist was scratched. The conducting path is probably going to be interrupted, meaning that this device will not be usable. Picture taken with the Optishot 200 with a magnification of 5x.

On chip 15 of wafer 7672, the photoresist was apparently scratched after the coating or the developing (Figure 19).

3.1.3 Etching

The bottom contacts were patterned with a dry etching performed in the *STS multiplex ICP* (standing for Inductively Coupled Plasma). The principle of etching is the following : a plasma is initiated with a radio-frequency magnetic field. Charges and ions are moving around in the chamber and electrons deposit on the wafer, building up a negative potential. The positive ions then tend to drift toward the wafer, colliding and etching the surface, both chemically by reacting with the surface molecules and physically by sputtering.

The recipe *AlN_etch* was used for all three materials. In this recipe, chlorine (flow of 20 sccm) was the chemical component and *Ar* was the physical element (flow of 5 sccm). This etching was performed with platen and coil powers of 175 W and 800 W respectively.

A table summarizing the etching rates in the *STS* is available (Table 2). As it gave us a first approximation of the total etching time we needed to run, we did not follow it blindly for different reasons. First, we could not be certain of the actual thicknesses of material deposited by the *Pfeiffer SPIDER 600*. Second, the reproducibility of the etching rates of the *STS* has never proved to be stable (possibly also because the thicknesses of the layers were not well controlled). Following the table, the recipe AlN_etch should be run for a 113 seconds to remove all the three layers of interest (20 nm of SiO_2, 25 nm of Pt and 15 nm of AlN successively).

Material	**Recipe**	**Etching rate**
Platinum	AlN_etch	$\approx$ 25 nm/min
Aluminum nitride	AlN_etch	$\approx$ 250 nm/min
Silicon dioxide	AlN_etch	$\approx$ 70 nm/min

Table 2: Etching rates for contact materials with recipe AlN_etch.

Additionally to being challenging to control, the etching rates in the STS are not uniform over the wafer. Indeed, the *STS* is etching the center of the wafer slower than the borders. Some areas are therefore going to be slightly over-etched to ensure that the target layers are removed everywhere. The experience has shown that the best strategy is to start with a 50-second etching, and then proceed with steps of 10 seconds until the etching is complete.

Two methods are applicable to determine whether an etching was finished. The simpler is the eye-test : the visual appearance of the wafer changes as layers are removed. A more conventional and precise method is to use end-point detection. Before starting the process, a laser spot is focused on an area on the wafer that is going to be etched. The light is reflected, collected and then processed by an external software. Observing the signal informs about the state of the etching.
An additional technique can be used if we are dealing with metallic layers. Probing areas on the wafer with a multimeter is a simple test to know whether a metallic layer has been removed. That is the method we adopted.

Wafer 7672 was etched for 50 seconds. Unloading it and checking the resistance between two theoretically insulated points with a multimeter, we obtained an an overload value. The

platinum layer had therefore been completely removed. The possibility existed that a thin layer of aluminum nitride would remain on the wafer. Nevertheless, due to the very fast (250 nm/min) etching of that material, we did not process the wafer further to avoid damaging the underlying silicon nitride.

As the processing of wafer 7672 seemed complete, it was decided for safety to slightly reduce the etching time down to 45 seconds for wafer 7674. Unloading the wafer after this initial step and checking the resistance between two points that were supposed to be insulated, we noticed conductance. Therefore, we reloaded the wafer and proceeded to continue to etch. Successive etching steps of 6, 8, 5, and 10 seconds were performed. After each step, the wafer conductivity was quickly measured before reloading for a new run. In the end, it took a total of 74 seconds of AlN_etch to entirely remove the target layers, which was in great contrast with the 50 seconds necessary for the previous wafer, and not even close to the theoretical 113 seconds. We noticed that during the 5-second etch, the plasma was actually operating only for about 2 seconds. Therefore, performing many short etching steps removes less material than a single equally long step.

3.1.4 Photoresist strip

The first step of photoresist removal is oxygen plasma. The wafers were put in the *Tepla 300*, an oxygen dry etcher with high frequency plasma, and the recipe Strip_High was run for 5 minutes. Afterwards, the wafers were placed for 5 minutes in each of the two remover 1165 baths heated at 70°C. Then, they went through 3 runs of Cascade Tank (fine rinsing), skipping the usual Quick Dump Rinse step which is much stronger and could damage the microchannels. At the end, an isopropyl alcohol (IPA) bath was added to clean the wafer and prevent the membranes from stitching.

3.1.5 Oxide strip

The silicon dioxide layer was removed in a 7:1 BHF solution. One minute was sufficient to remove the entirety of the 20-nm-thick SiO_2 layer, since the etching rate of silicon oxide had been measured to be 75 nm/min. The channels top walls consist of thin silicon nitride membranes (about 1.5 μm thick). To prevent collapse and stiction of such membranes to

the bottom of the microfluidic channels, we were careful to always leave the wafer in liquid. The best approach for rinsing and drying was thus to use a second recipient already filled with water in which the wafer could be put immediately after the BHF etching. Then this recipient could be emptied and filled as many times as needed to rinse thoroughly. Before being left to dry, the wafer was put in an isopropyl alcohol (IPA) bath. The high volatility of this compound helped avoiding collapse of the silicon nitride membranes. This IPA bath was an extra step added as extreme precaution. Indeed, the presence of pillars inside the channels should be sufficient to support the membranes and prevent collapse.

A conductivity check was then conducted to ensure that the oxide had been entirely removed. Probing the resistance between two points on the same pad, we obtained a resistance in the tens of Ω, confirming the success of the oxide strip.

Then, we used the scanning electron microscope to have a deeper look at our devices. In particular, we checked for the presence of fences. Fences are undesired structures which result from the redeposition of etched material at the edges of the features during dry etching processes. Their formation during platinum dry etching is a well known phenomenon [24]. In our case, if the fences were too high and stiff, they could cause short circuit between bottom and top electrodes after the deposition of the top contact, described in 3.2.
Figures 20 and 21 show SEM pictures of the bottom contacts on wafer 7672. We notice the presence of fences on the sides of the electrodes.

Zooming on those features (Figures 22 and 23), it could be assessed that they would not cause short-circuit issues with the top contact, because they are folded on the platinum pad and not free standing. Indeed, the following deposition of a 300-nm-thick aluminum nitride layer on top of the bottom contact would ensure insulation between the metallic parts of each contact.

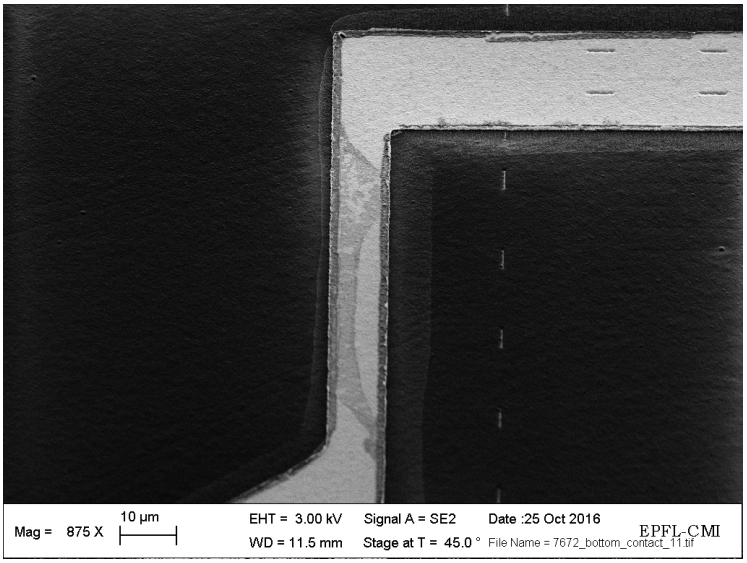


Figure 20: Bottom contact on a chip of wafer 7672. We notice the presence of fences at the sides of the electrode. Picture taken with the SEM.

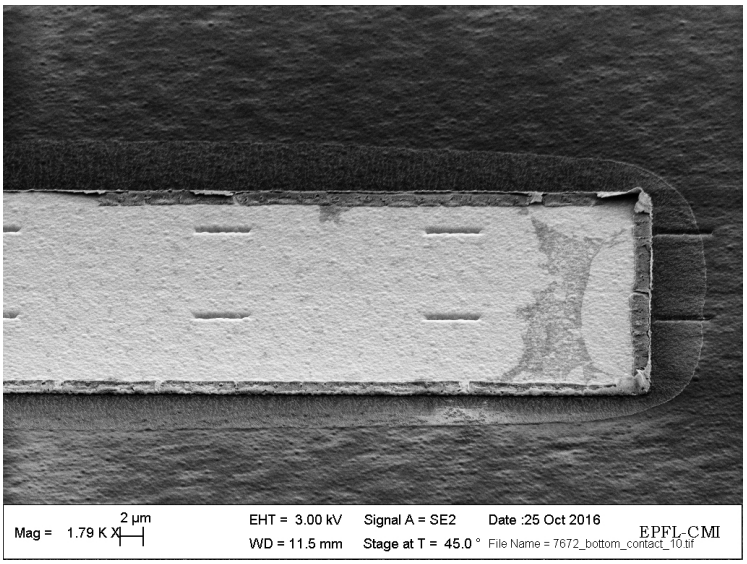


Figure 21: Ending of a bottom electrode of wafer 7672. We clearly see fences falling onto the platinum at the corners of the electrode. The horizontal apertures used to remove the inside of the channels are visible as well. Picture taken with the SEM.

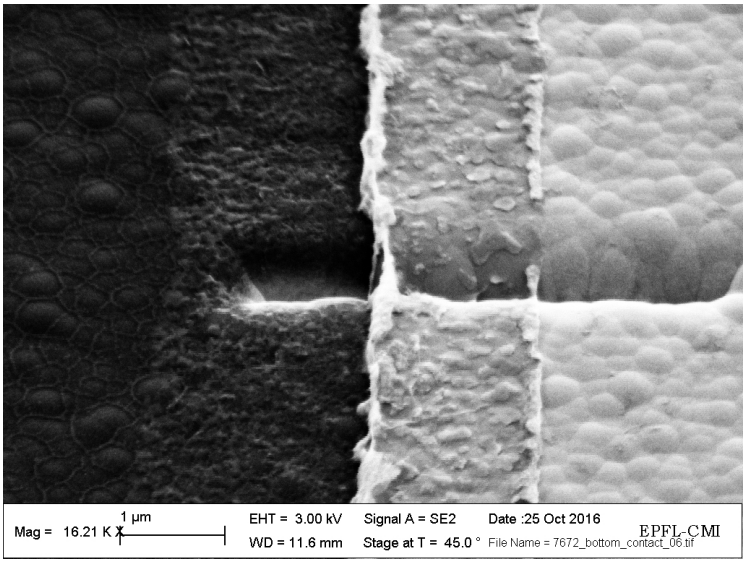


Figure 22: Edge of a bottom electrode of wafer 7672 that happens to overlap an aperture. Picture taken with the SEM.

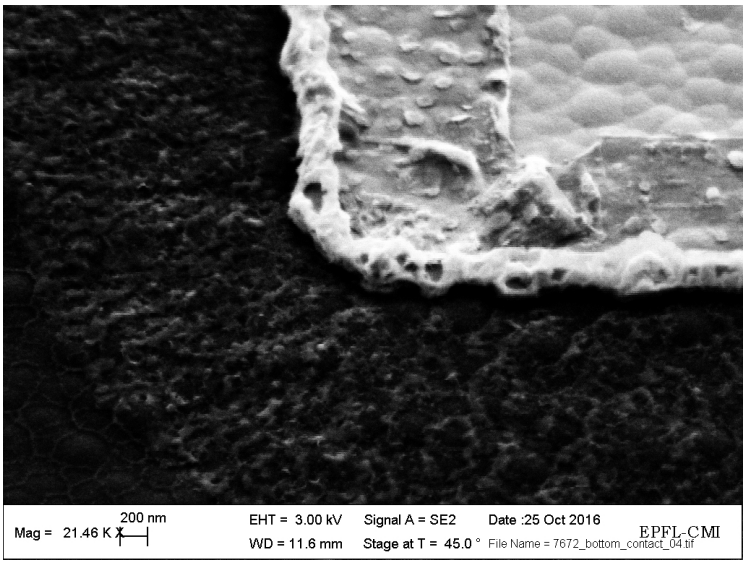


Figure 23: Corner of a bottom electrode of wafer 7672 exhibiting fences. Picture taken with the SEM.

3.2 Top contact

3.2.1 Sputtering

The second layer of aluminum nitride, underneath the top electrode, is much thicker than the first layer. Indeed, it is the layer that is going to act as the piezoelectric material for both the actuation and the detection. A thicker layer of material could be beneficial to achieve higher performance, but it would also increase the mass and stiffness of the device. This is undesirable since the device is going to be employed as mass and stiffness sensor.

300 *nm* of aluminum nitride, 25 *nm* of platinum, and 20 *nm* of silicon dioxide were sputtered in the *Pfeiffer SPIDER 600*. To clean the targets and check the reflective power, we used the exact same procedure as for the first deposition (3.1.1).

The details of the parameters for this deposition are listed in Table 3.

Again, we checked with a multimeter that the silicon dioxide had been correctly deposited.

Slot	ID	Task	Recipe	Step	T [°C]	Time	Thick.	Power [W]	sccm
25	dum.	SiO_2 clean	SiO2 clean target	1	RT	-	-	1000	-
23	dum.	*Pt* clean	Pt_T_clean_target_350	1	300	-	-	1000	-
21	dum.	*AlN* prep	AlN_prep_350	1	300	-	-	1500	-
21	dum.	RP check	AlN_T_D1	2	300	5:00	-	1500	40/10
19	7672	*AlN*-300nm	AlN_T_D-2_Pt_T_D-2_Etch_D-2	3	300	6:00	300nm	1500	40/10
		Pt-25nm			300	0:06	25nm	1000	-
17	7674	*AlN*-300nm	AlN_T_D-2_Pt_T_D-2_Etch_D-2	3	300	6:00	300nm	1500	40/10
		Pt-25nm			300	0:06	25nm	1000	-
19	7672	SiO_2-20nm	SiO2_F-1	4	RT	1:00	20nm		
17	7674	SiO_2-20nm	SiO2_F-1	4	RT	1:00	20nm		

Table 3: Parameters used for the deposition of the top contact

3.2.2 Photolithography

For the photolithography of the top electrodes, both wafers were coated with 2 μm of AZ ECI 3027 positive photoresist (*ACS200* program 0326).

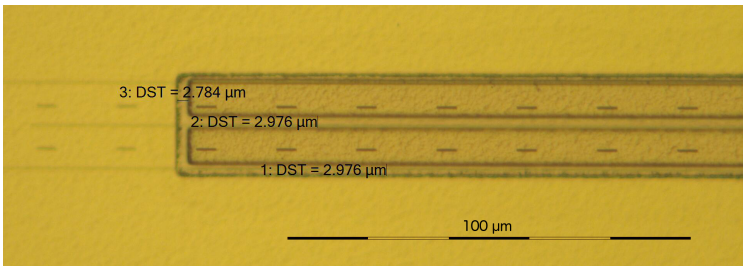
The wafers were then exposed with *MLA150* with a dose of 150 mJ/cm^2 and a defocus of -3.

The wafers were developed in the *ACS200* (program 0926) and the alignment was further checked with the optical microscope.

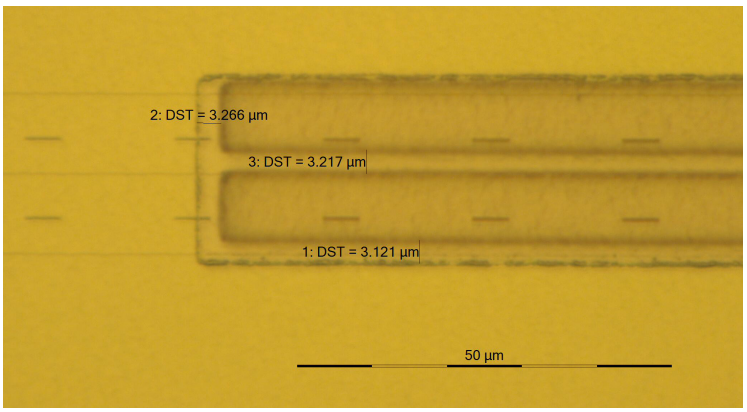
Figure 24 shows optical microscope pictures of the cross alignments for the top contact on wafer 7674. The horizontal alignment seems good, but a better result could possibly have been achieved in the vertical direction. Indeed, the crosses are slightly closer to the top squares than to the bottom ones.
Having a closer look at the patterned photoresist, we notice that the cross misalignments reproduced on the electrodes features. On chips 7 and 16 (pictured by Figures 25a and 25b), we clearly see that the two fingers representing the top contacts are not centered with respect to the underlying bottom contact. This effect seemed accentuated on chips located on the lowest row of the wafer, such as chip 16. The explanation was that the furthest vertically away from the center the devices were, the strongest the effect of the initial misalignments. Although the misalignment was noticeable and rather significant, it should not turn out to be problematic, because the top electrodes were still well enclosed within the bottom contact.
Figure 26a depicts the smallest features found on the wafer, found on chip 1. We notice that the top electrodes are defined adequately, and that the dimensions are very close to the 2 μm expected from the CleWin design (Figure 26b).

(a) Left cross *(b) Right cross*

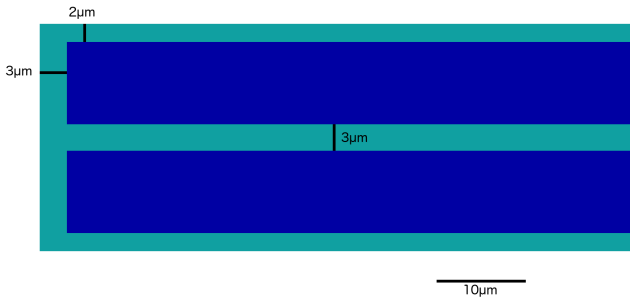
Figure 24: Alignment of the top contact mask on the bottom contact mask (4 to 3 alignment marks) on wafer 7674. We notice that both crosses are slightly higher than they should. Nevertheless, the alignment was ruled as successful. Pictures taken with the Optishot 200 microscope, with a magnification of 20x.



(a) Features measurements of top contact photoresist on chip 7 of wafer 7674. The misalignment is rather small. Picture taken with the Optishot 200 microscope with a magnification of 50x.

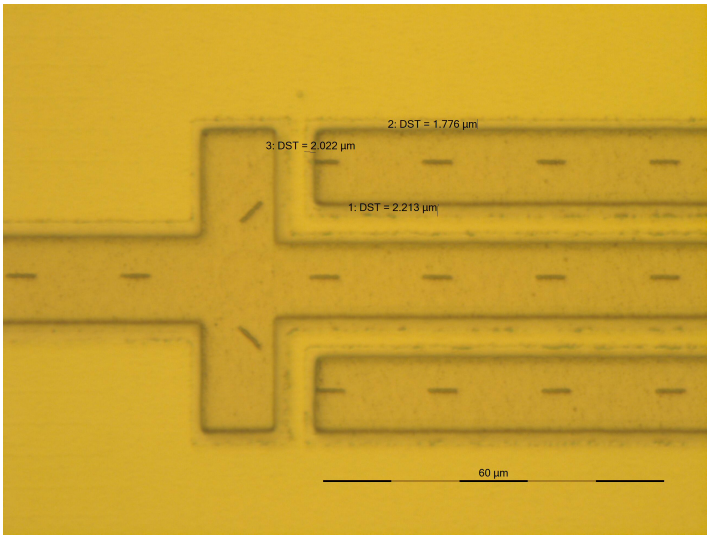


(b) Features measurements of top contact photoresist on chip 16 of wafer 7674. The misalignment is more pronounced as the chip is on the lowest row of the wafer. Picture taken with the Optishot 200 microscope with a magnification of 100x.

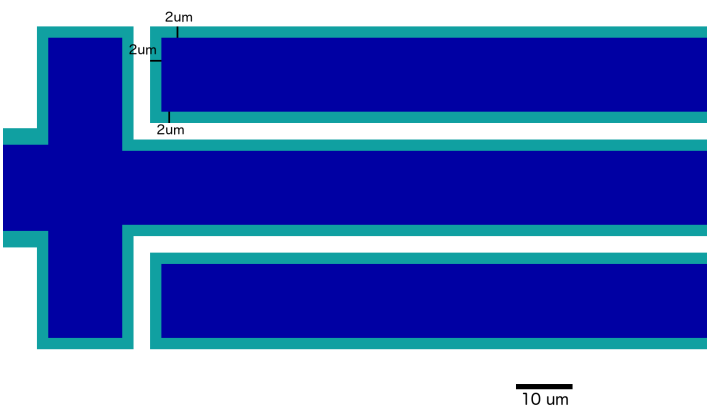


(c) Theoretical features of the top electrodes as designed in CleWin.

Figure 25: Photoresist features on different chips of wafer 7674. We notice that the dimensions are close to those expected from the design.



(a) Smallest photoresist features for the top contact (on chip 1 of wafer 7672). We notice a nearly perfect alignment with the bottom electrode. Picture taken with the Optishot 200 microscope with a magnification of 100x.



(b) Corresponding features sizes as designed in CleWin.

Figure 26: Comparison of the actual result of the photolithography with the CleWin design for the smallest top electrodes features (chip 1).

3.2.3 Etching

The top electrodes were patterned in the *STS* by running the same recipe as for the etching of the bottom contact : AlN_etch. According to Table 2, we expected the etching to be about 2' long.

As we could not follow the etching rates to define the duration of a recipe, we decided to start with 1'50". Additionally, and similarly to what was achieved for the bottom contact, further etchings could be added to complete the process if needed.

The first wafer to be processed was 7674. After etching for a duration of 110 seconds, we took the wafer out to check the resistances. We measured values in the range of 20 Ω on the same pads of bottom electrodes. This means that we reached the platinum layer of the bottom contact, and that etching of the top layers was already complete.

Processing the wafer 7672 for the same duration of etching, we noticed the resistances were different depending on the chip checked. We measured 17 Ω on the left-side contacts of chip 1, a chip located on the first row, and 180 Ω on the right-side contacts of that same chip. In contrast, an overload resistance on electrodes of chip 9, a chip located at the center, was measured, indicating that the etching was not finished. Therefore, we run an additional 12-second step. Surely, it etched the platinum of the bottom electrode on some chips in the border of the wafer, but to negligible thicknesses. Checking again with a multimeter the platinum of the bottom electrodes of the same chips, the resistance was still 20 Ω on the left-side of chip 1, but now 17 Ω on the right-side of chip 1, and more importantly, 16 Ω on chip 9.

3.2.4 Photoresist and oxide strip

To strip the photoresist and the oxide, we proceeded with the exact same procedure as previously described for the bottom contact (see Section 3.1.5).

Once the oxide was removed, a series of electrical measurements were performed at the *PM8* probe station. In order to avoid damaging the electrodes of the chips, the characterization was conducted on test structures located on the sides of the wafer. The layout of a complete

test structure is sketched in Figure 27. The resistances measured between different pads on wafer 7674 are summarized in Table 4.

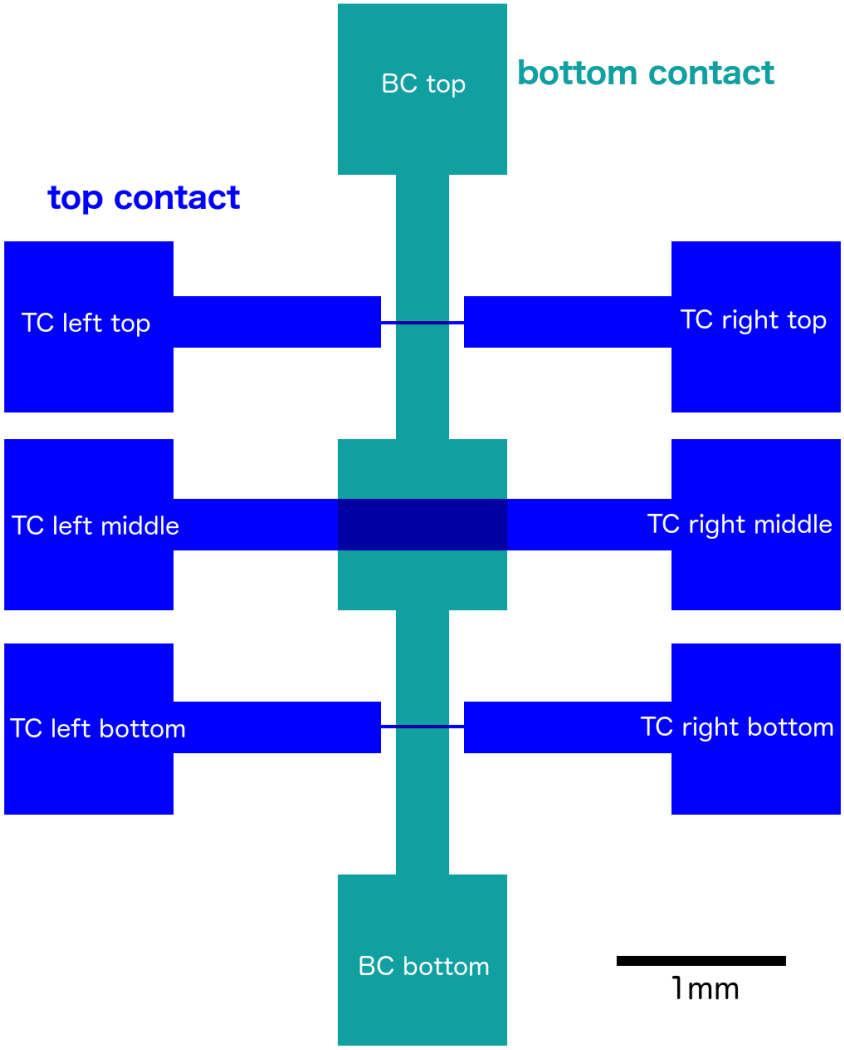


Figure 27: Layout of the test structure and naming of the pads.

Probing two connected top contacts separated by a reduced electrode width, such as between TC left top and TC right top, yielded resistances in the hundreds of Ωs. If the electrode path was larger (such as between TC left middle and TC right middle), the resistance was lower than 100 Ω. This can be simply explained by the resistance being inversely proportional to

the cross-section of the electrode, as stated by the well-known equation :

$$R = \rho \cdot \frac{l}{A} \tag{1}$$

where

ρ : electrical resistivity $[\Omega \cdot m]$

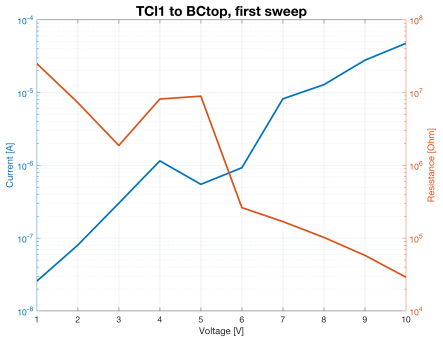
l : length of the conductor $[m]$

A : cross-sectional area of the conductor $[m^2]$

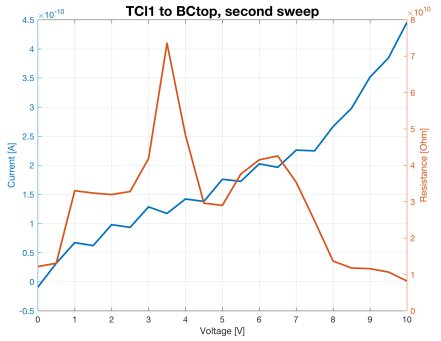
Pad 1	**Pad 2**	**Measured resistance**		
		at 1 V	**at 2 V**	**at 4 V**
TC left top	BC top	190.75 $M\Omega$	42.64 $M\Omega$	788.59 $k\Omega$
TC right top	BC top	208.36 $M\Omega$	68.69 $M\Omega$	8.53 $M\Omega$
TC left top	TC right top	376 Ω	383 Ω	405 Ω
TC left bottom	BC bottom	39.86 $M\Omega$	12.78 $M\Omega$	1.49 $M\Omega$
TC right bottom	BC bottom	231.55 $M\Omega$	73.86 $M\Omega$	11.74 $M\Omega$
TC left bottom	TC right bottom	364 Ω	369 Ω	385 Ω
TC left middle	TC right middle	85 Ω	86 Ω	86 Ω
BC top	BC bottom	75 Ω	75 Ω	76 Ω

Table 4: Resistances measured between different pads of the test structure of wafer 7674. We notice a general satisfactory behaviour, with some exceptions (TC left bottom to BC bottom exhibit very low values). Additionally to those tests, probing the resistance between two points on the same pad always lead to values between $15 - 40$ Ω.

The resistance between the top and the bottom electrodes, ideally infinite, was measured in the hundreds of $M\Omega s$ for an applied voltage of 1 V. As the voltage increased, the resistance diminished. Nevertheless, keeping a voltage below 4 V should ensure proper operation of the devices. At higher voltages, the measured resistances reached breakdown, quickly dropping or skyrocketing, hinting at device failures. In other words, the electrodes became unusable. For example, on wafer 7672, a high voltage was applied between the TC left top and BC top pads. The behaviour was correct up to 5 V (slow decrease of the resistance in the range



(a) Voltage sweep between the top and bottom electrode of wafer 7672. We notice a breakdown at 5 V.



(b) Voltage sweep on the same structure after breaking down. We notice resistance values in the $G\Omega$. The device was therefore irreversibly damaged.

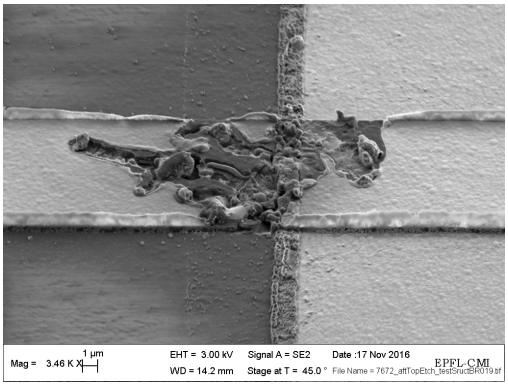
Figure 28: Voltage sweeps and effect of breakdown on a structure of wafer 7672.

of the tens of $M\Omega$). Then, the resistance increased steeply (Figure 28a). After running a second characterization between the same pads, the resistance was measured in the $G\Omega$, much higher than the previous values (Figure 28b). We guessed that we broke the contact by applying a voltage too high.
We continued the characterization on the remaining operational pads keeping the voltage low enough and did not notice any unexpected behaviours.

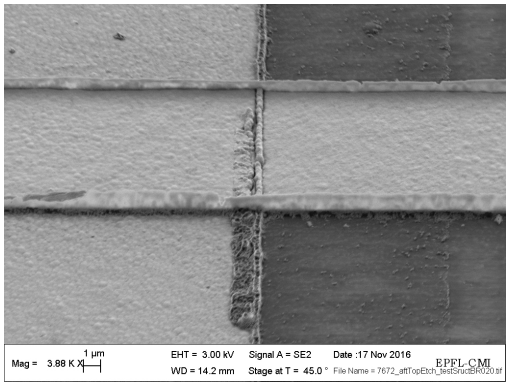
Following the electrical characterization, we looked at our devices with the SEM to check the deposition of the top contact. The wafer observed was 7672.

We started by having a look at the test structures. Figure 29a shows the damaged contact between the TC left top and BC top. The assumption that the connection was destroyed because of the high voltage applied is verified. As a comparison, Figure 29b depicts an operational contact.

Figure 30 depicts two top electrodes overlapping a bottom electrode. We see that the etching was generally complete on the electrodes area. Nevertheless, aluminum nitride remained on the silicon nitride. In Figure 31, we zoomed closer to the region of overlapping. The deposition of the top electrode was altered by the underlying border of the bottom electrode.



(a) Damaged top contact after application of a high voltage between the top contact and the bottom contact pads. We see that the connection is interrupted, leading to an open circuit.



(b) Operational top contact.

Figure 29: Comparison between a damaged and an operational top contact overlapping a bottom contact. Pictures taken with the SEM.

Although this frontier is clearly seen, it should not impede the subsequent operation of the devices. We notice some residues falling from the top electrode onto the bottom contact. Figure 32 depicts other residues linking the top to the bottom electrode. As it was charaterized that the top and bottom contact were insulated from each other, we concluded that those residues were not conducting. They were likely carbon-based compounds originating from the photoresist. Figure 33 shows the area between two top electrodes. We notice that the area has been well etched, avoiding any detrimental contact between the electrodes.

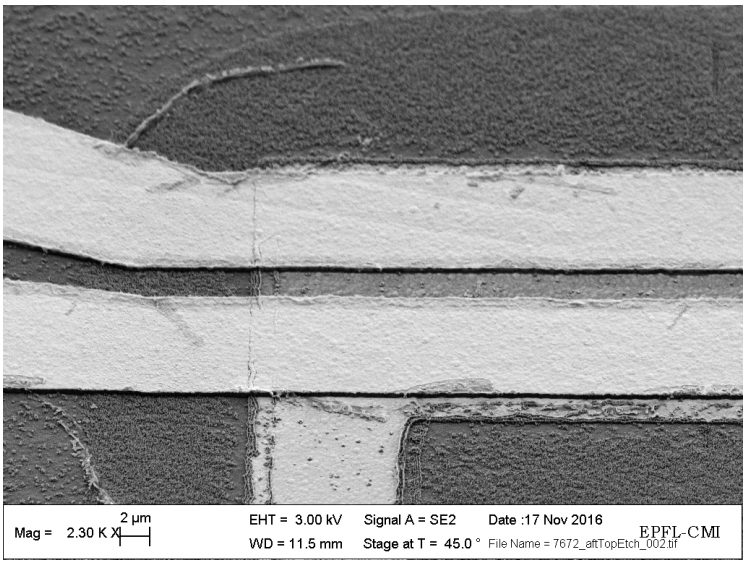


Figure 30: Two top electrodes overlapping a bottom electrode on waver 7672. The etching is generally complete on the electrodes, but there is still AlN remaining around. Picture taken with the SEM.

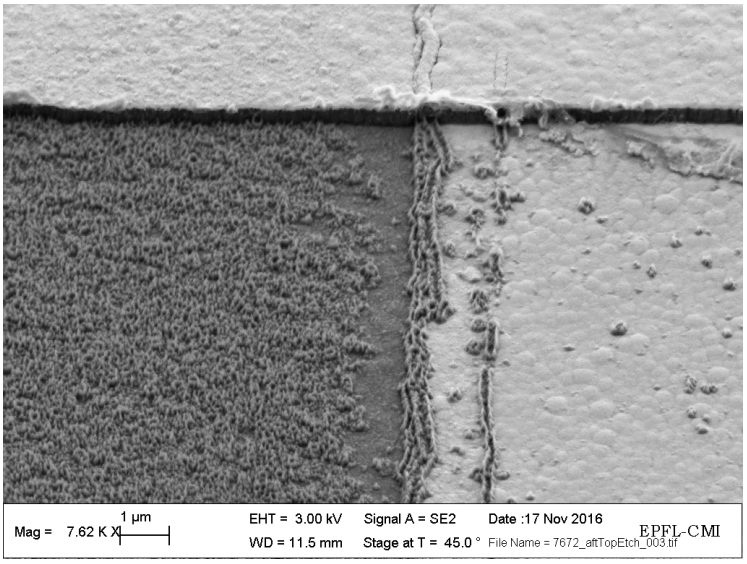


Figure 31: Closer look at the overlapping between the contacts. We still see the border of the bottom electrode on the top platinum, but it should not impede the device to operate properly. Picture taken with the SEM.

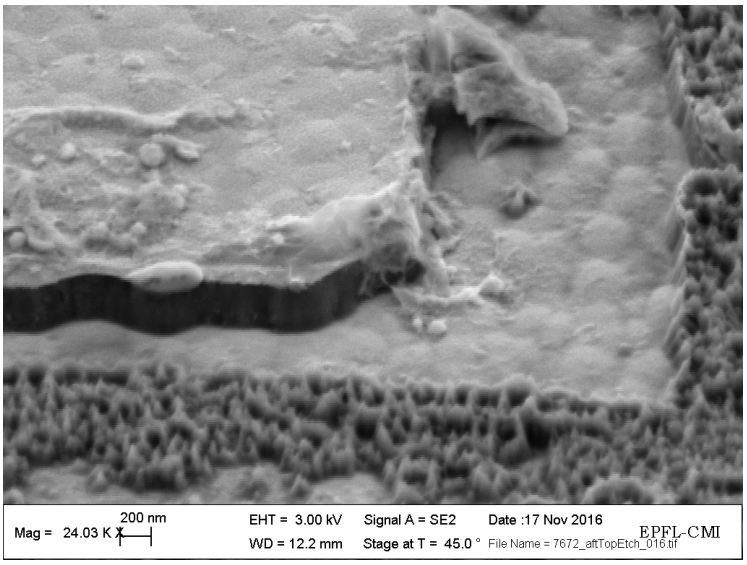


Figure 32: Residues falling from the top electrode and linking to the bottom contact on wafer 7672. Measured insulation between the top and bottom contact indicated that those residues were not conductive, but are some organic-based compound originating from the photoresist. Picture taken with the SEM.

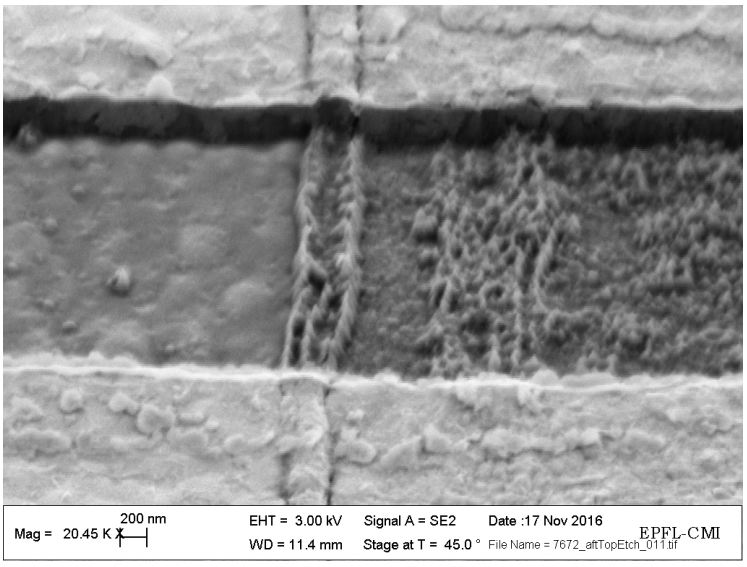


Figure 33: Area separating two top electrodes on wafer 7672. Wee see that the region is properly etched and there are no contacts between the electrodes.

3.3 Poly-silicon islands

3.3.1 Photolithography

From this step on, we only processed the wafer 7672.

After the top electrodes were properly etched, we patterned the so-called poly-silicon islands. To actuate and sense the resonators in the best conditions, it is best to minimize parasitic capacitances. This can be achieved removing conducting material, such as poly-Si, between the electrodes. Figure 34 depicts a CleWin layout of the areas that are to be etched (in white).

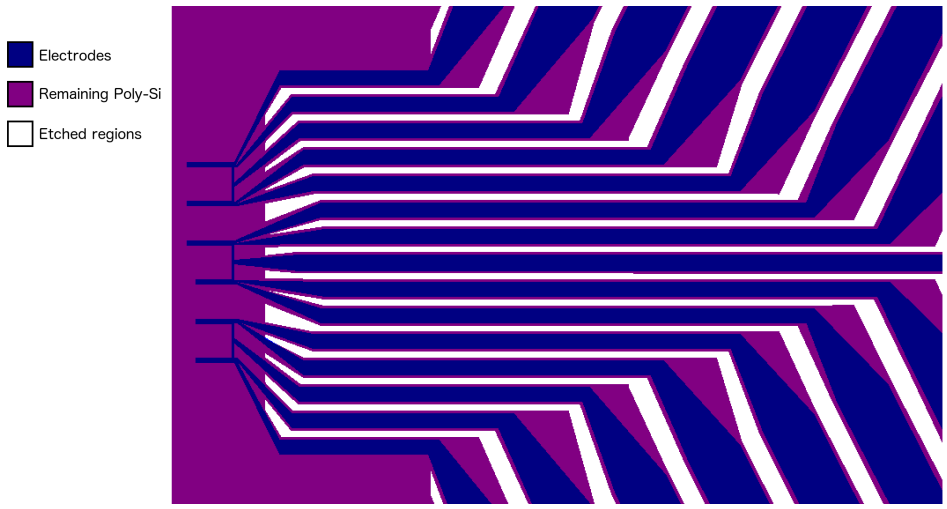


Figure 34: CleWin layout of the so-called poly-silicon islands (white areas are etched).

For this photolithography, we deposited 5 μm of AZ ECI 3027 with *ACS200* (program 0329). Then, with the *MLA150*, the designed was converted with the fast mode and exposed with a dose of 170 mJ/cm^2 and a defocus of -2. After development, we discovered that the wafer resulted in large areas of under-exposed photoresist, as shown in Figure 35. The wafer had to be stripped and the process to be started over.

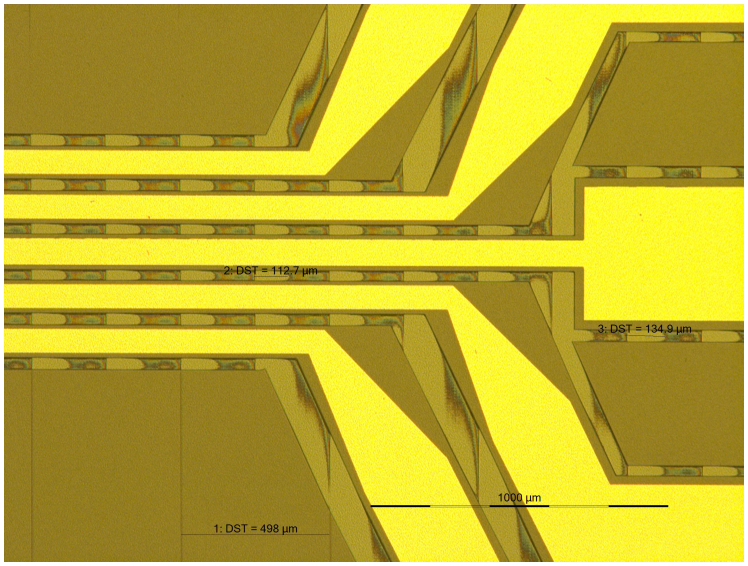
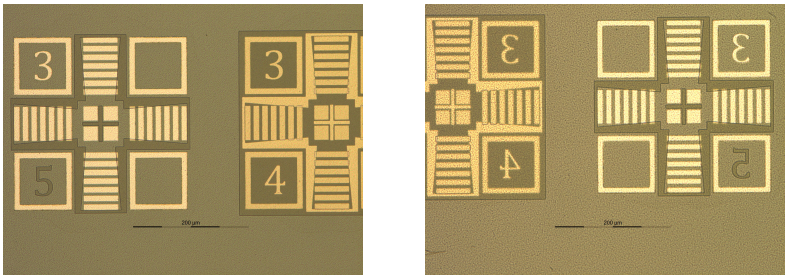


Figure 35: Under exposed photoresist on wafer 7672 after performing the poly-silicon island exposure with the fast mode conversion. Picture taken with the Optishot 200 with a magnification of 5x.

The second time, 3 μm of AZ ECI 3027 only were deposited with *ACS200* (program 0327). The parameters for the subsequent exposure with *MLA150* were a dose of 180 mJ/cm^2 with a defocus of -3 and a high quality conversion. The wafer was well exposed, and the alignment was successful, as depicted in Figure 36.



(a) Left cross *(b) Right cross*

Figure 36: Alignment of the poly-silicon island mask on the top bottom contact mask (5 to 3 alignment marks) on wafer 7672. We notice that both crosses are successfully aligned. Pictures taken with the Optishot 200 microscope, with a magnification of 20x.

3.3.2 Etching

Etching of the poly-silicon islands was performed with the *Alcatel 601E*, a Deep Reactive Ion Etching (DRIE) equipment. On wafer 7672, the etching targets were a layer of 1.4 μm of low-stress silicon nitride, and the underlying 6-μm-thick poly-silicon layer. With *Alcatel 601E*, the etching rates are well known and usually stable. They are listed in Table 5.

Material	**Recipe**	**Etching rate**
Silicon nitride	NITRURE_1	280-300 nm/min
Photoresist AZ ECI	NITRURE_1	300 nm/min
Poly-silicon	ADP_ANISO	4.5 μm/min
Photoresist AZ ECI	ADP_ANISO	130 nm/min

Table 5: Etching rates of recipes in Alcatel 601E.

We started with a 5' etching running recipe NITRURE_1, a continuous C_2F_6-based etching selective to poly-silicon, to remove the silicon nitride layer, and followed with 1'31" of ADP_ANISO to etch the poly-silicon. ADP_ANISO is a Bosch process : it is a pulsed etching made of a first active step of SF_6 (5", 300 sccm) and a second passivation step of C_4F_8 (2", 200 sccm). An optical microscope picture after those two processes is shown in Figure 37. We notice a repetition of vertical lines in the etched areas. The explanation is that those lines came from photoresist that was not properly removed after the first photolithography performed with the fast mode conversion writing in the *MLA*, and acted as a mask for the first seconds of etching (see Section 3.3.1). The periodicity of 250 μm in the line spacing seems to support this explanation. Indeed, it corresponds to the width of the stripes of the *MLA* : the exposure took about 400 stripes to write a wafer measuring 100 mm in diameter.

Monitoring those features with the *Dektak* mechanical profilometer, we learned that their height was around 2 μm (Figure 38a). Subsequently, we ran numerous etching processes and checked the evolution of those features both with the optical microscope and with the profilometer. Table 6 summarizes all the recipes, including the two initial etchings, performed as we tried to remove those lines of residues. As well, the table includes the evolution of the thickness of the photoresist, ensuring the safety of the process, and the

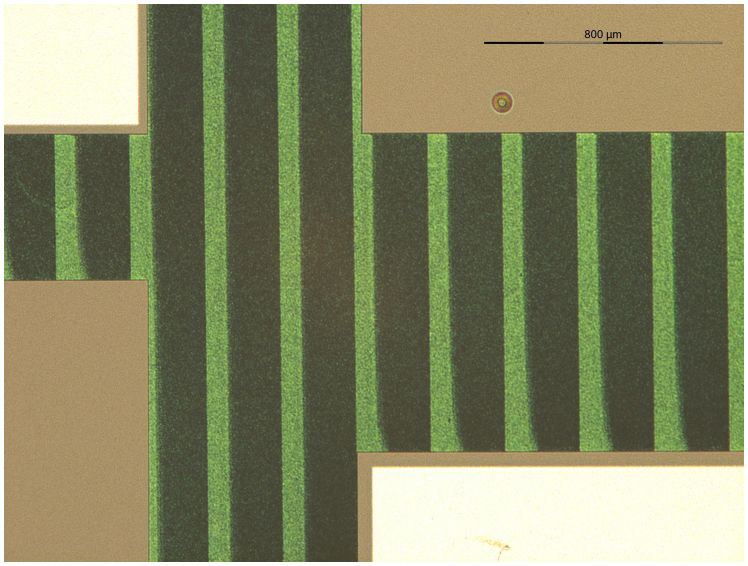
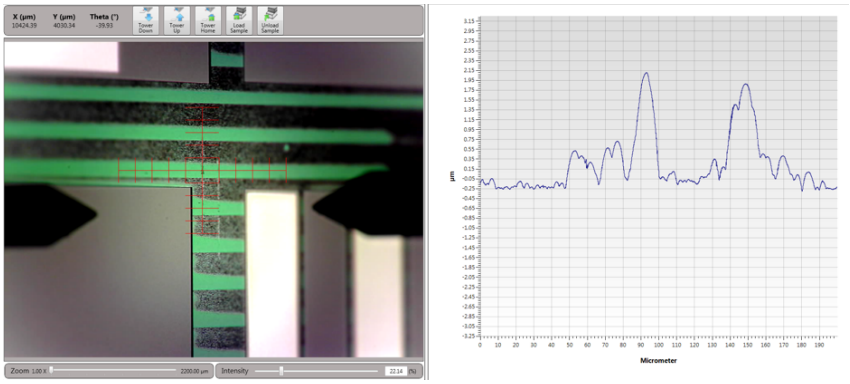


Figure 37: Vertical lines after etching of the poly-silicon islands. They are caused by photoresist residues from the previous photolithography. Picture taken with the Optishot 200 with a magnification of 5x.

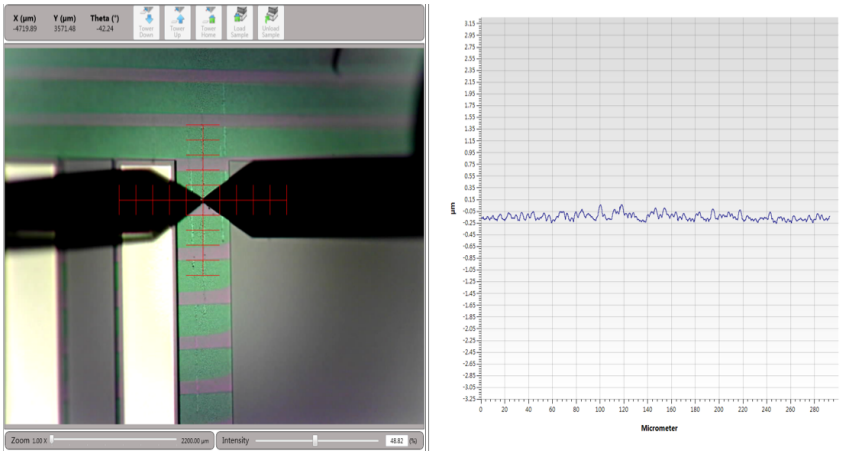
height of the residues as measured with the profilometer. We did not systematically measure those features at the exact same spot, which explains why the residues seemed removed after a process and were back to 2 μm later on. We guessed that the passivation layer (coming from the Bosch process) protecting the residues was being removed at different moments all over the wafer. With a combination of NITRURE_1 and ADP_ANISO recipes, we were not able to get rid of the features : according to the profilometer, the largest residues were still about 2 μm high.

The residues could finally be minimized running 1 minute of a SF_6-based silicon isotropic dry etching, (SI_RELEASE recipe of *Alcatel 601E*). This step was safe because the etching of photoresist with SI_RELEASE is very slow (5 nm/min). This process allowed us to considerably reduce the poly-silicon residues (Figure 38b), because the SF_6 gas helped removing the passivation layers preventing the etching. Nevertheless, as can be seen in Figure 39, the features are still visible.

The *Nanospec* tool optically measured a remaining 350 nm-thick layer of silicon nitride on the bottom, meaning that we overetched the bottom nitride, originally 500 nm thick.



(a) After the initial NITRURE_1 and ANISO_ADP recipes, there are residues left on the surface, with an approximate height of 2 µm.



(b) After 1' of SI_RELEASE, the surface is measured as nearly flat. The residues height was greatly reduced.

Figure 38: Screenshots of the profilometer measurements performed with the Dektak profilometer. We notice that the colour of the features changed.

Recipe	Duration	Photoresist left	Residues height
		3.000 μm	
NITRURE_1	5'00"	$-1.5 = 1.500$ μm	
ANISO_ADP	1'31"	$-0.2 = 1.300$ μm	
ANISO_ADP	10"	$-0.022 = 1.278$ μm	5 μm
NITRURE_1	10"	$-0.06 = 1.218$ μm	
ANISO_ADP	1'10"	$-0.152 = 1.066$ μm	100 nm (center of wafer)
ANISO_ADP	10"	$-0.022 = 1.044$ μm	
ANISO_ADP	20"	$-0.044 = 1.000$ μm	1 μm
ANISO_ADP	1'00"	$-0.132 = 0.868$ μm	2 μm

Table 6: Etching steps performed at the Alcatel 601E to define the poly-silicon islands.

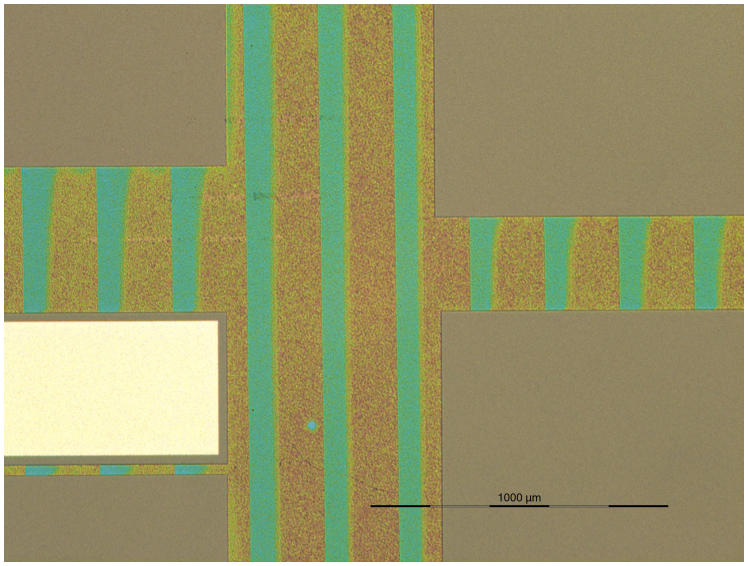


Figure 39: The vertical features are still visible at the optical microscope even after the surface was confirmed to be flat at the profilometer. Picture taken with the Optishot 200 with a magnification of 5x.

The wafer was then observed with the SEM to check how the residues actually looked like. Figure 40 clearly shows the lines that we already saw with the optical microscope. As can

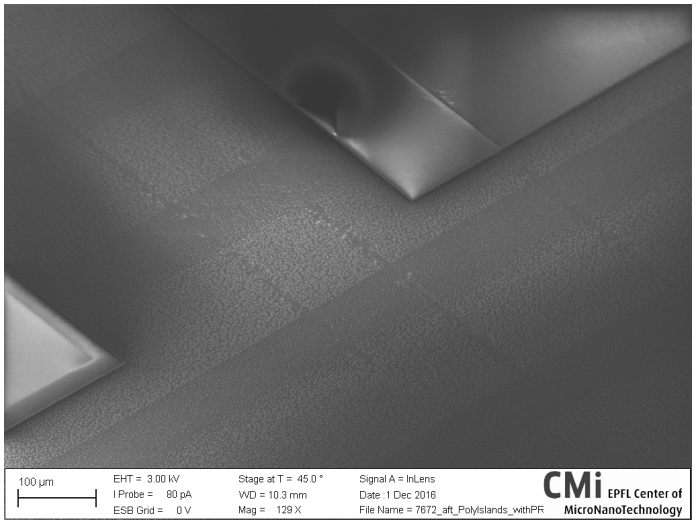


Figure 40: Periodic vertical lines imaged with the scanning electronic microscope.

be seen on a picture with higher magnification (Figure 41), the residues seemed too tiny and dispersed to create a conductive path between two electrodes. We could thus expect that the parasitic capacitance would be kept to a minimum due to the absence of poly-silicon between electrodes.

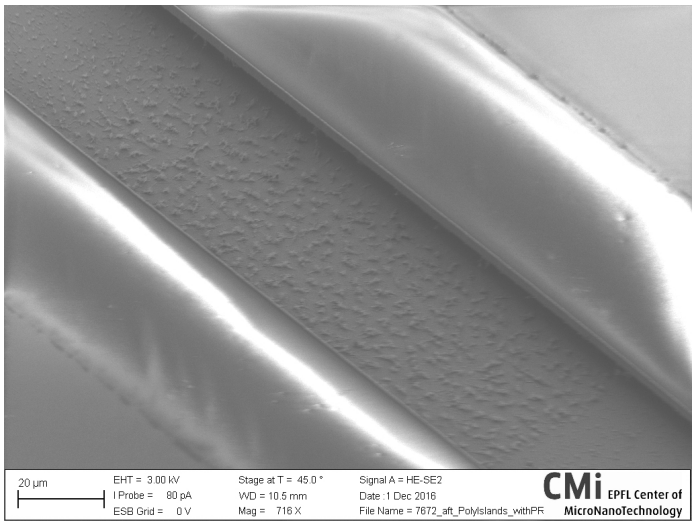


Figure 41: The residues seem too small and remote from each other to achieve a conductive path between two electrodes. The parasitic capacitances should therefore be minimized. Picture taken with the SEM.

3.3.3 Photoresist strip

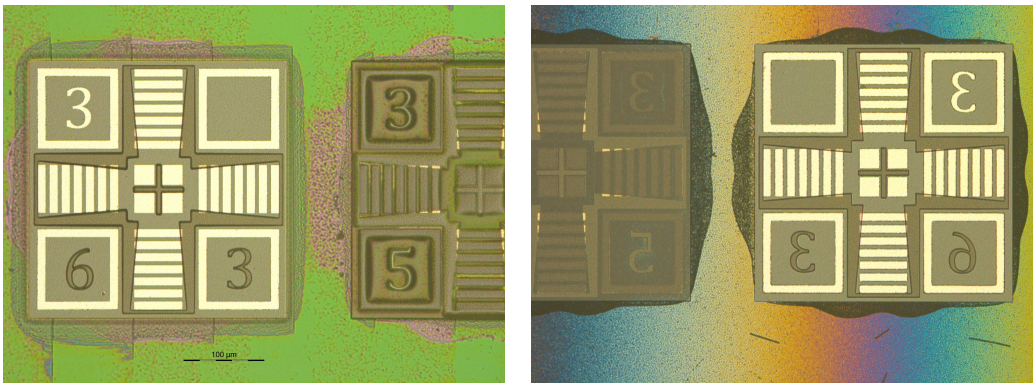
A standard procedure followed to strip the photoresist. The wafer was exposed to an oxygen plasma in *Tepla 300* for 5 minutes with the recipe $Strip\_High$. It followed 15 minutes in each bath of remover, and 3 runs of cascade cleaning. In the end, a 3-minute $Strip\_Low$ recipe was added. Probing electrodes with a multimeter confirmed that the photoresist had been successfully removed.

3.4 Cantilever release and inlet openings

3.4.1 Photolithography

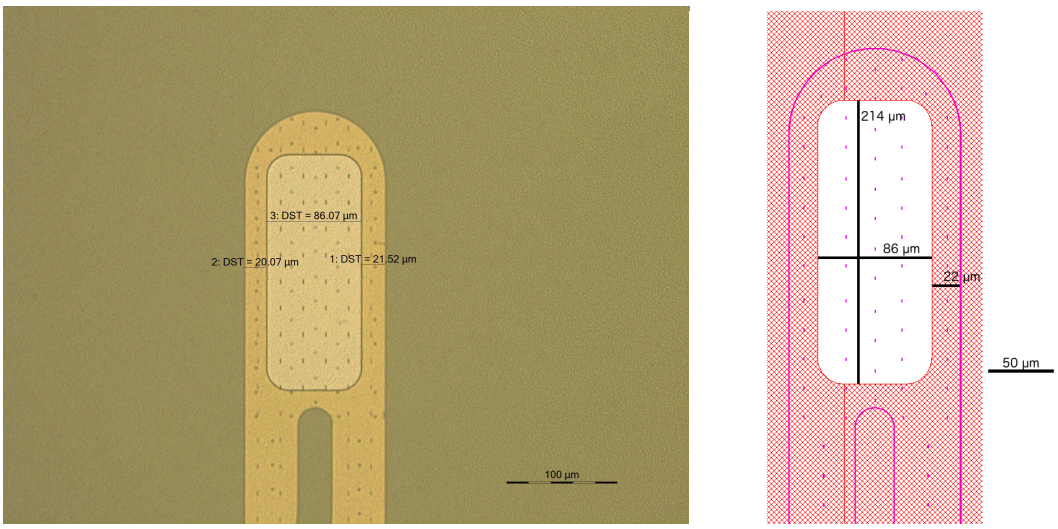
For the final lithography of the process flow, we coated the wafer with 5 μm of AZ ECI photoresist (*ACS200*, program 0329). The *MLA* parameters were a dose of 230 mJ/cm^2 and a defocus of -3, exposing a design that was converted with high quality. The wafer was then developed in the *ACS200* with program 0929, and Figure 42 depicting the crosses shows that the alignment was excellent.

Figure 43 compares the features sizes of an inlet opening on chip 2 with the CleWin design. Even though the positioning tolerance of the inlet openings with respect to the underlying channels were not crucial, we see that they were well centered. The alignment of the photoresist area protecting the cantilever during the release was much more critical. We compared the results obtained on two chips (2 and 10) with respect to the CleWin design in Figure 44. On chip 10, the alignment was impeccably centered, whereas on chip 2, the photoresist was slightly misaligned. Nevertheless, we see that it entirely covered the channels and even exceeded them on each side by more than 1.5 μm, the required margin to also enclose the electrodes at the clamping.



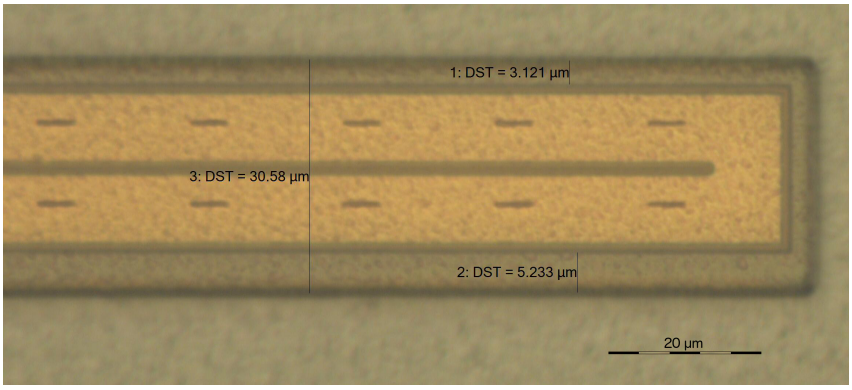
(a) Left cross *(b) Right cross*

Figure 42: Alignment of the cantilever release mask on the top bottom contact mask (6 to 3 alignment marks) on wafer 7672. We notice that both crosses are remarkably aligned. Pictures taken with the Optishot 200 microscope, with a magnification of 20x.

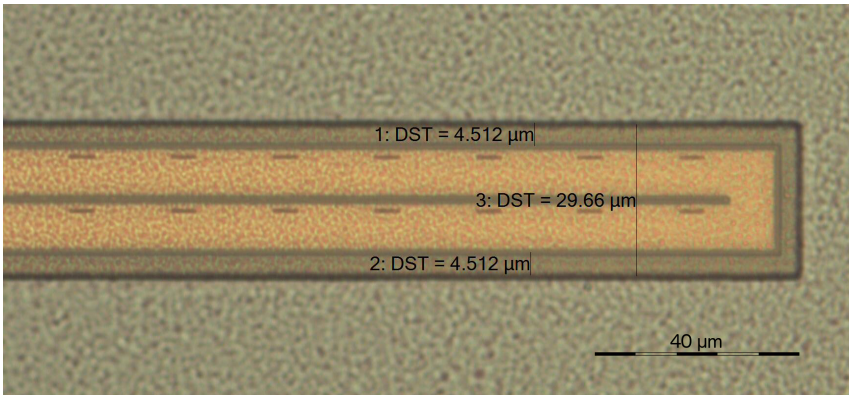


(a) Alignment of the photoresist features. Picture taken with the Optishot microscope with a magnification of 20x. *(b) CleWin design*

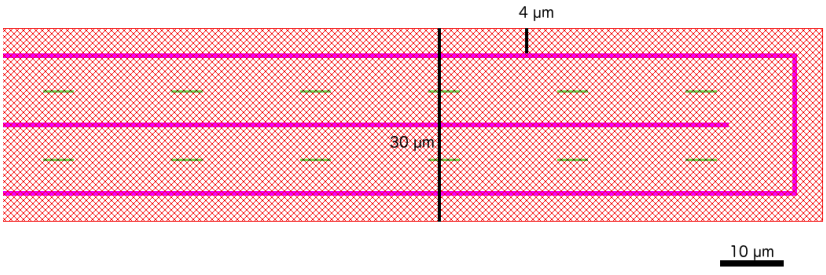
Figure 43: Comparison between the photoresist features and the theoretical CleWin design of an inlet on chip 2. We notice that the photoresist was perfectly patterned. Pictures taken with the Optishot 200 microscope, with a magnification of 20x.



(a) Alignment of the photoresist on top of a cantilever of chip 2. We notice a slight misalignment. Nevertheless, the photolithography was successful because the dimensions measured are well within the margins tolerated. Picture taken with the Optishot microscope with a magnification of 100x.



(b) Perfect alignment of the photoresist on top of a cantilever of chip 10. Picture taken with the Optishot microscope with a magnification of 50x.



(c) CleWin design

Figure 44: Comparison between the photography features of the release and the CleWin design.

3.4.2 Etching

The final part of the process flow consisted in releasing the resonators and opening the inlets. The first steps were identical to the etching of poly-silicon islands: we removed the top layer of silicon nitride (1.4 μm) and the layer of poly-silicon (6 μm). Additionally, we removed the bottom layer of silicon nitride (500 nm), and etched downward the silicon for about 10 μm with a Bosch process to make the subsequent release faster. The first three recipes were configured to last slightly longer than the planned etching time to ensure that the target layers were completely removed.

The release strictly speaking was achieved by a SF_6-based silicon dry etching recipe labelled SI_RELEASE. After an initial step of 5 minutes, we checked the wafer at the microscope. Figure 45, showing the state of a cantilever on chip 8, is misleading. On one hand, we could clearly observe a shadow around the cantilevers, hinting that the release has started. On the other hand, we noticed that the top silicon nitride appears in two different colours: the greyish colour on the sides of the cantilever was identical as in the substrate on the left of the picture, where no material had been removed. In contrast, the reddish colour seemed to indicate an absence of material underneath. Not being entirely convinced that the release was complete and willing to avoid a costly SEM inspection, we decided to add additional etching steps (8 minutes of SI_RELEASE in total). As resist had not been completely consumed, no silicon nitride was directly exposed to SF_6, so those processes should not damage the channels.

Figure 46 shows cantilevers of chip 8 after the additional 8 minutes of release. We noticed that the reddish area had propagated and even reached the channels on the left of the picture. Therefore, our assumption that the mentioned reddish area represented underlying etched material could be confirmed. In addition to that, we noticed that same colour on the sides of the cantilevers. The release undoubtedly progressed, and was likely complete.

Figures 47 and 48 depict SEM views of complete chips, confirming the smooth execution of the release process.

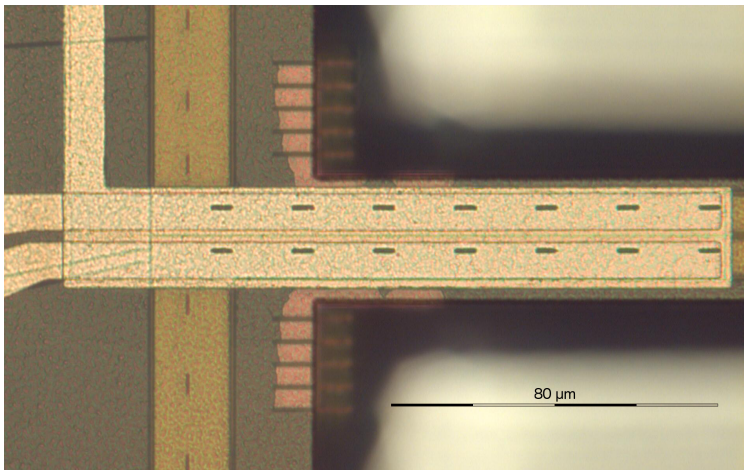


Figure 45: A cantilever on chip 8 of wafer 7672 after the initial release steps. We notice the different colours on the sides of the cantilever, hinting at the fact that the poly-silicon was not removed everywhere. Picture taken with the Optishot 200 with a magnification of 50x.

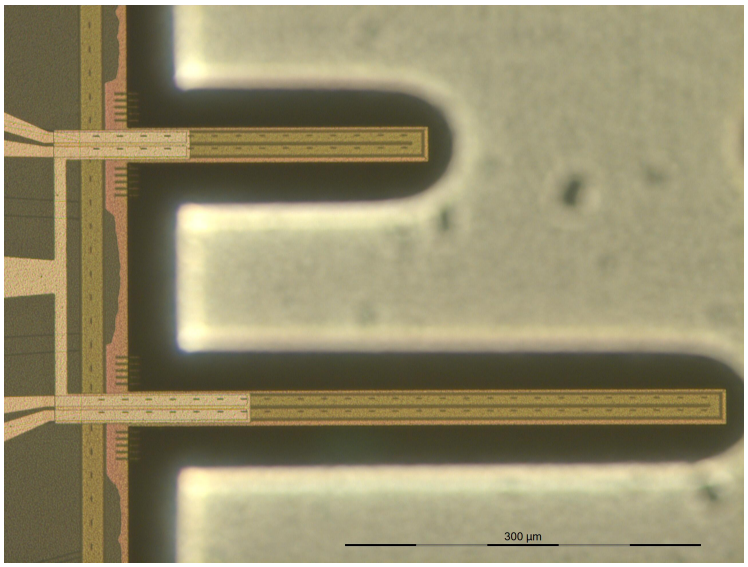


Figure 46: Cantilevers on chip 8 of wafer 7672 after additional release steps for a total of 8 minutes. The structure are likely to be completely released. Picture taken with the Optishot 200 with a magnification of 20x.

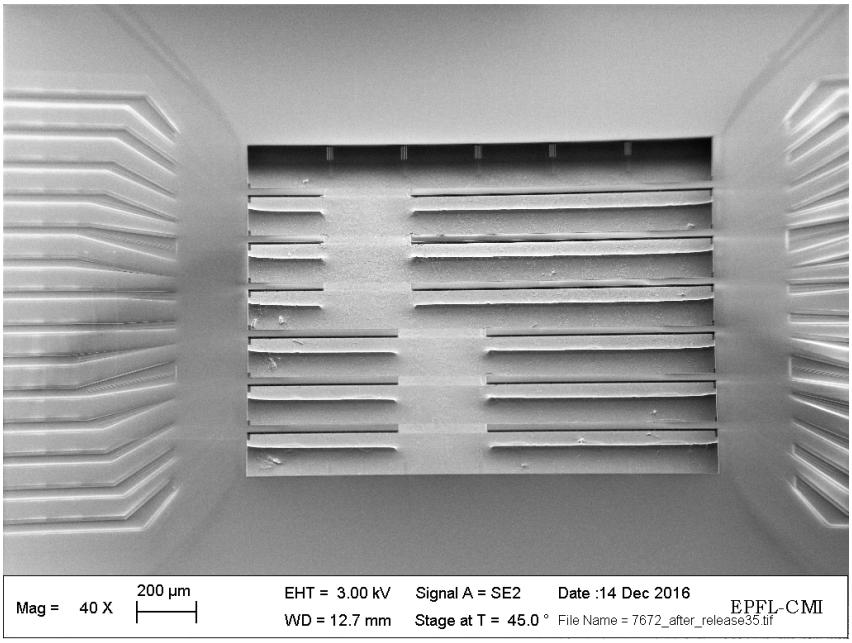


Figure 47: Chip with completely released cantilevers. Picture taken with the SEM.

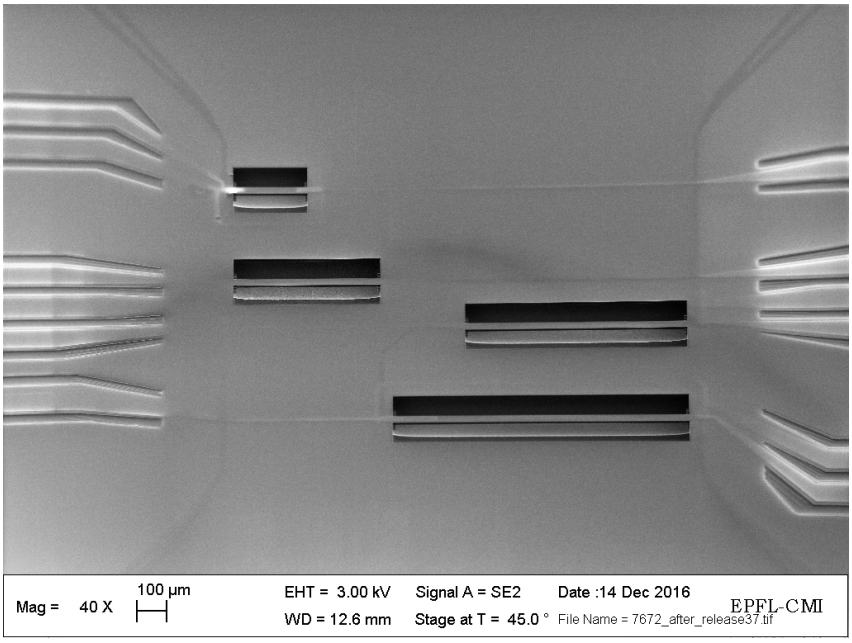


Figure 48: Chip with completely released beams. Picture taken with the SEM.

After completion of the release, we observed rings of material at the end of some cantilevers. Those features arised from the filling of the apertures designed to facilitate the etching of the interior of the channels by KOH. As some cantilevers were not closed by a silicon nitride wall at their end (Figure 49), KOH was not constrained to the inside of the channels and happened to etch the poly-silicon around the cantilevers. After the channels had been emptied, the apertures were filled with silicon nitride by chemical vapour deposition. In the beginning of the process, the gas entered the channels and deposited on the walls. In the cantilevers missing their end wall, silicon nitride happened to deposit further on the surface of the poly-silicon cavity defined. Figure 50 shows a detailed image of one of those rings taken with the SEM. With the objective of removing those features, we later performed more silicon nitride etching steps at the *Alcatel 601E*. As a comparison, Figure 51 depicts a properly defined cantilever.

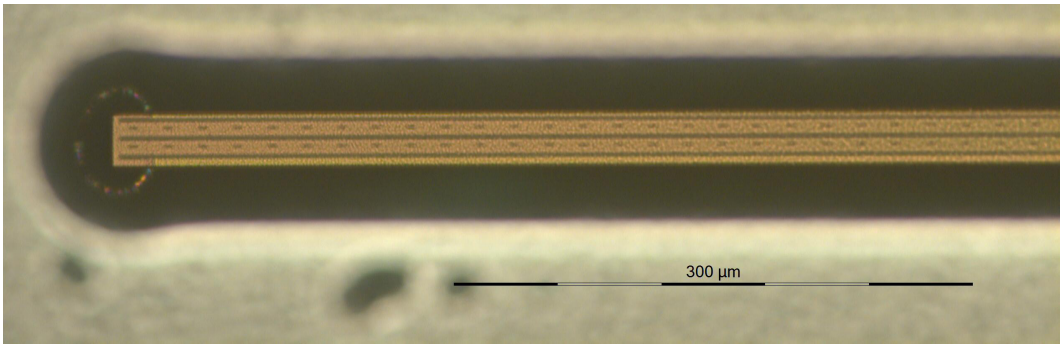


Figure 49: Presence of a ring of silicon nitride around the end of the cantilever. It is arising from the aperture filling silicon nitride deposition following the KOH etching. As the cantilever was not properly closed at the end, gas could propagate and deposit on walls much further than the cantilever. Picture taken with the Optishot 200 with a magnification of 20x.

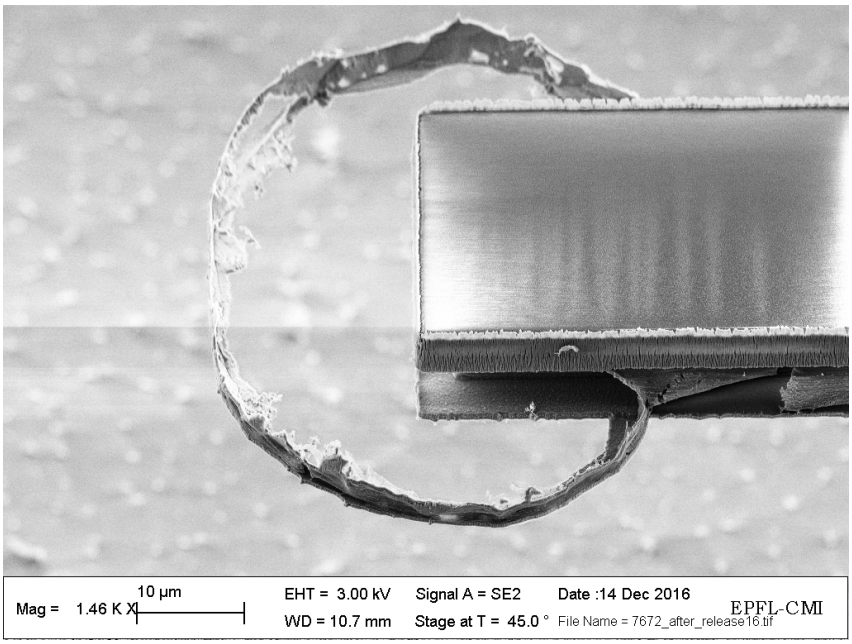


Figure 50: Silicon nitride ring at the end of a cantilever. Picture taken with the SEM.

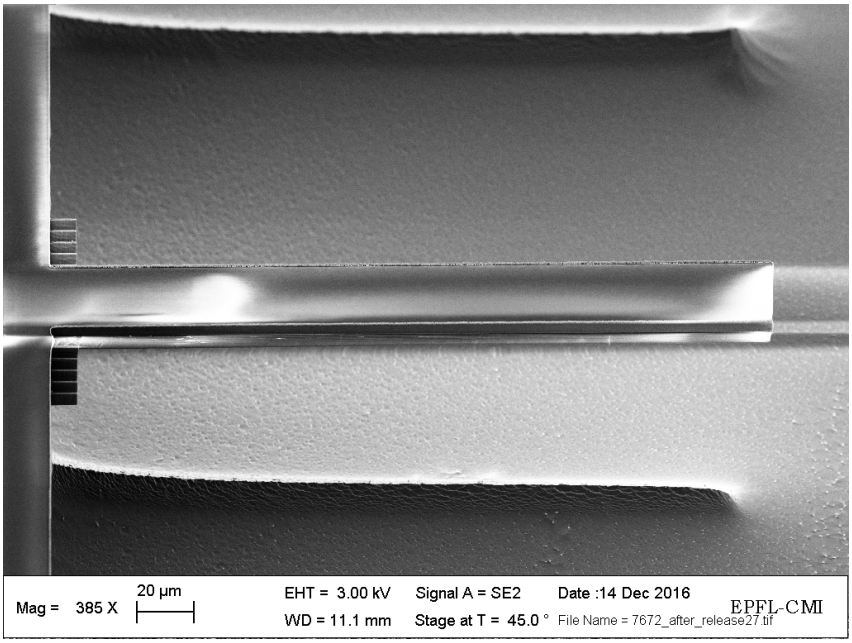


Figure 51: Cantilever released. As it did have a silicon nitride wall at its end, this cantilever did not have any ring attached.

The focus was then set on trying to remove the silicon nitride rings. As can be seen in Table 7, which summarizes all the steps performed for the release, we processed the wafer in 4'30" of NITRURE_1 and 1' of ANISO_ADP. As pictured in Figure 52, we were successful in removing the bottom part of the rings. However, as their height was likely close to the poly-silicon layer thickness (6 μm), most of the vertical part of the rings remained. Nevertheless, some rings were severely affected by the etching and happened to break at some locations, leaving only a fragment of the previous feature (Figure 53). At that point, we did not rule out the possibility that the entirety of the silicon nitride rings could be removed with the actuation of the cantilevers.

Recipe	**Planned duration**	**Actual duration**	**Photoresist left**
			5.000 μm
NITRURE_1	5'00"	5'30"	$-1.650 = 3.350$ μm
ANISO_ADP	1'31"	1'38"	$-0.212 = 3.138$ μm
NITRURE_1	2'00"	2'10"	$-0.650 = 2.488$ μm
ANISO_ADP	2'30"	2'30"	$-0.325 = 2.163$ μm
SI_RELEASE	5'00"	5'00"	$-0.025 = 2.138$ μm
SI_RELEASE	-	3'00"	$-0.015 = 2.123$ μm
SI_RELEASE	-	3'00"	$-0.015 = 2.108$ μm
SI_RELEASE	-	2'00"	$-0.010 = 2.098$ μm
NITRURE_1	-	3'00"	$-0.900 = 1.198$ μm
NITRURE_1	-	1'30"	$-0.450 = 0.748$ μm
SI_RELEASE	-	1'00"	$-0.010 = 0.738$ μm

Table 7: Etching steps performed at the Alcatel 601E to release the resonators and open the inlets.

Even if only the top silicon nitride layer would have needed to be removed to ensure access to the channels, all the processes enumerated were performed on the inlet openings. Although it created a significant cavity at the entrance of the channels, leading to a non negligible dead volume, this strategy allowed us to use a single lithography for both the inlets opening and the resonators release. Separating those two tasks into different processes would have

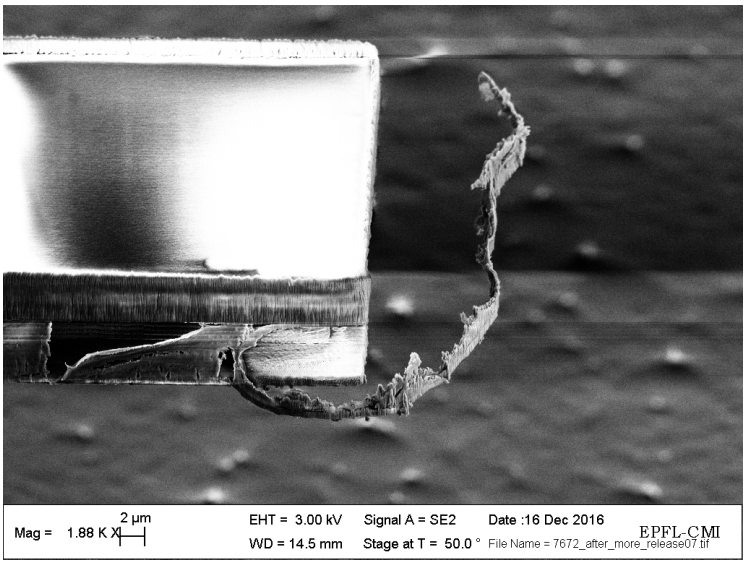


Figure 52: Ring attached to the cantilever after more etching of silicon nitride. We see that the bottom part of the ring was removed, but not the vertical walls. Picture taken with the SEM.

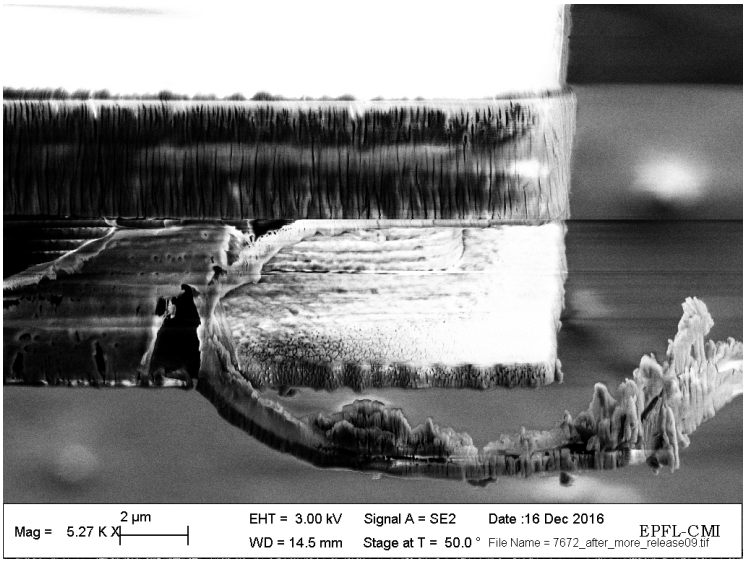


Figure 53: After more silicon nitride etching, it was possible to remove completely parts of the rings at some locations. Here the ring is only attached on one side of the wafer. Picture taken with the SEM.

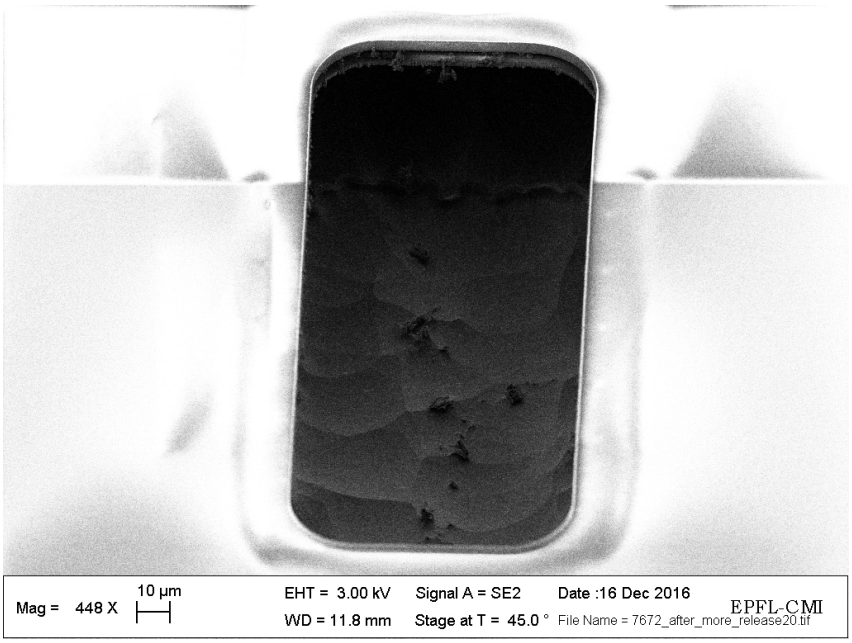


Figure 54: Inlet opening at the end of the process. Picture taken with the SEM.

been complex. If the release was performed first, photoresist would subsequently require to be coated on the cantilevers. We could hardly conceive of the success of such a process. On the other hand, if the openings of the inlets were defined first, photoresist would then be filling those cavities. Additionally to the probable challenging stripping of the photoresist at the end of the process, it was also highly likely that some of it would flow into the channels, eventually causing irreversible damages. For those reasons, release of the devices and inlets openings took place at the same time, and with the same processes. Figure 54 depicts an inlet opening at the end of the etching.

Observing the end of longer cantilevers, we noticed that the photoresist had been completely removed and that the top silicon nitride layer had started to be etched (Figure 55). The explanation for a quicker consumption of the photoresist at the end than at the clamping could lie in the heat transfer. Near the clamping of the cantilevers, metallic layers ensure a rather quick heat flow. In contrast, in the end of long cantilevers, it is more difficult to cool the photoresist down. The photoresist could thus be etched at different rates depending on the location on the cantilever. Although the cantilevers appeared seriously damaged (Figure 56), it was conceivable that they could still be operated and tested, because the top layer

of silicon nitride was rather thick.

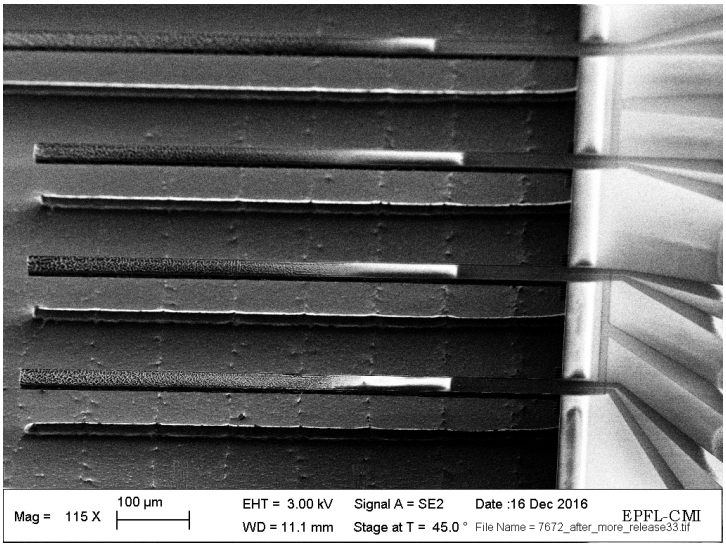


Figure 55: Longer cantilevers showed extensive areas of their protective photoresist completely consumed. The top silicon nitride was consequently etched. Picture taken with the SEM.

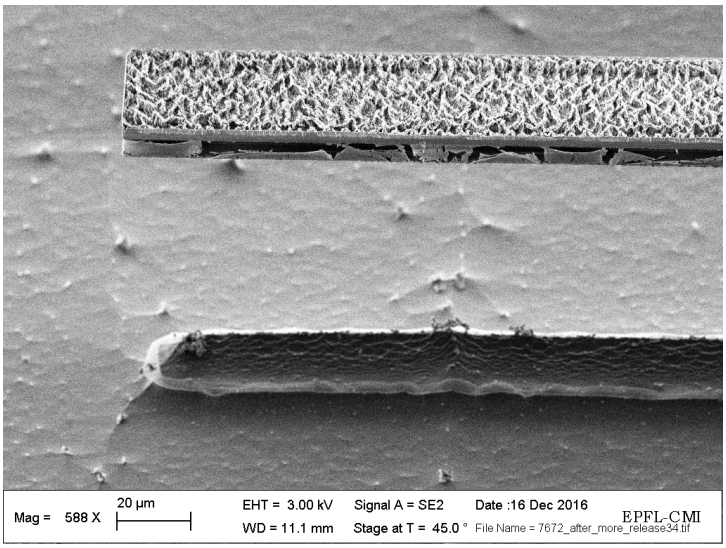


Figure 56: State of an etched cantilever with higher magnification. Because of the large thickness of the top silicon nitride layer, it is possible that the device could still be operated. Picture taken with the SEM.

3.4.3 Photoresist strip

Stripping the resist was the final step to execute before our wafer could be cleaved. As putting the wafer in remover baths was highly discouraged to avoid a potential collapse and stiction of cantilevers, we tried to process it in oxygen plasma alone. Running a variety of *Tepla* recipes (3' *Strip_Low*, 5' *Strip_High*, 3' *Strip_Low* and 15' *Strip_High* successively), we could completely remove the photoresist deposited on top of the devices.

Observing the devices with the SEM, and in particular chip 5 (in Figure 57 and in more detail in Figure 58), we remarked a few disturbing features. First, some residues of aluminum nitride remained on the top of the resonators. Additionally, fences were noticeable all around the top surface edges. Finally, we took note of the presence of partially detached layers on the sides of the devices. Those features likely originated from the passivation step of the Bosch process, which would explain the difficulty to remove them.

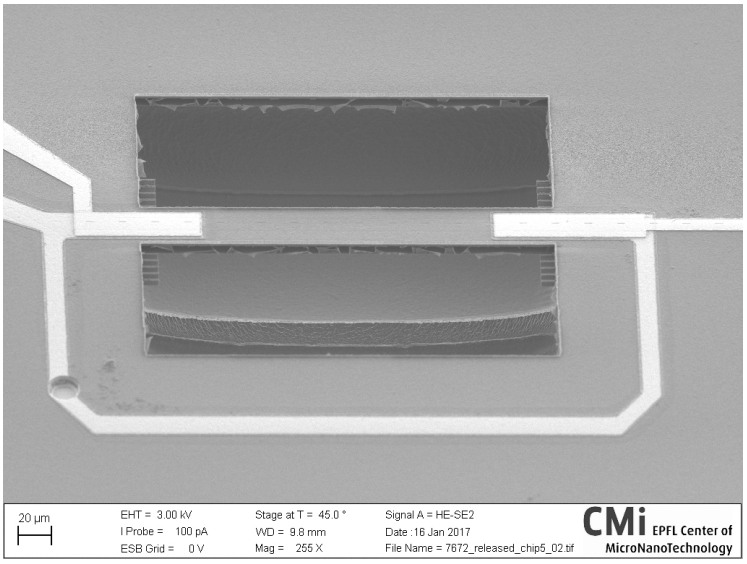


Figure 57: Chip 5 of wafer 7672 after processing in oxygen plasma. Picture taken with the SEM.

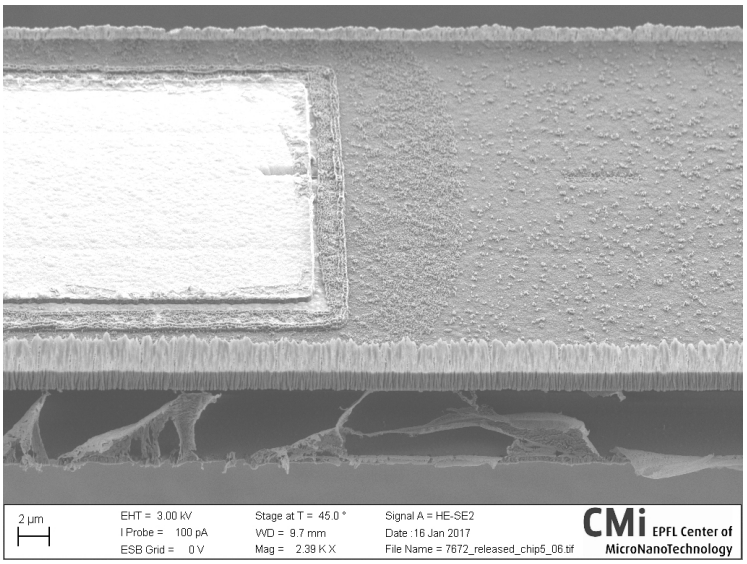


Figure 58: Zoom on undesired features on chip 5 of wafer 7672. We notice residual aluminum nitride on the top surface, fences all around the edges and a passivation layer on the sides of the device. Those features could not be removed in oxygen plasma. Picture taken with the SEM.

Performing an additional 15' *Strip_High* recipe did not have any impact on removing the undesirable features enumerated in the previous paragraph. We thus cleaved chip 5 and put it a KOH bath for about 5 seconds. Chip 5 being made of beams (resonators attached on their both sides), there was no risk of collapse and stiction of the devices if we put them in a bath. It turned out that this step yielded exceptional results. As can be seen in Figure 59, in addition to remove the residual aluminum nitride, we could get rid of both the fences and the lateral passivation layers.

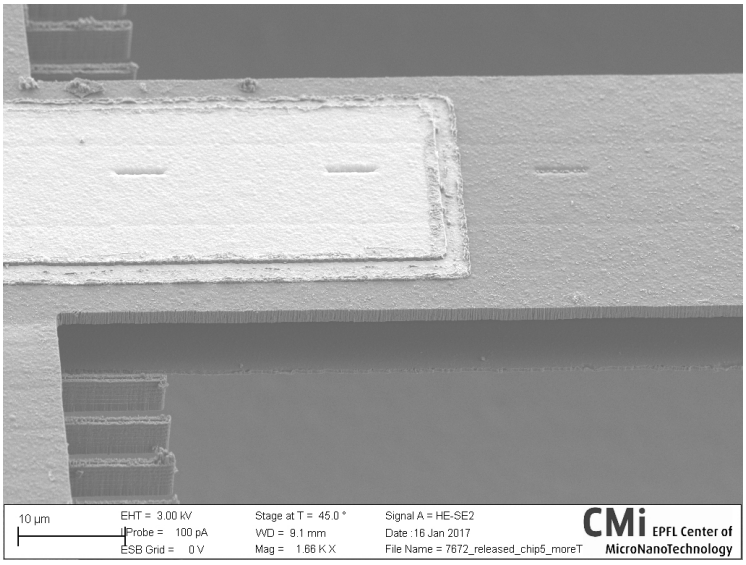


Figure 59: Chip 5 of wafer 7672 in its final state, after all the undesired features were removed. Picture taken with the SEM.

4 Microfluidic interface

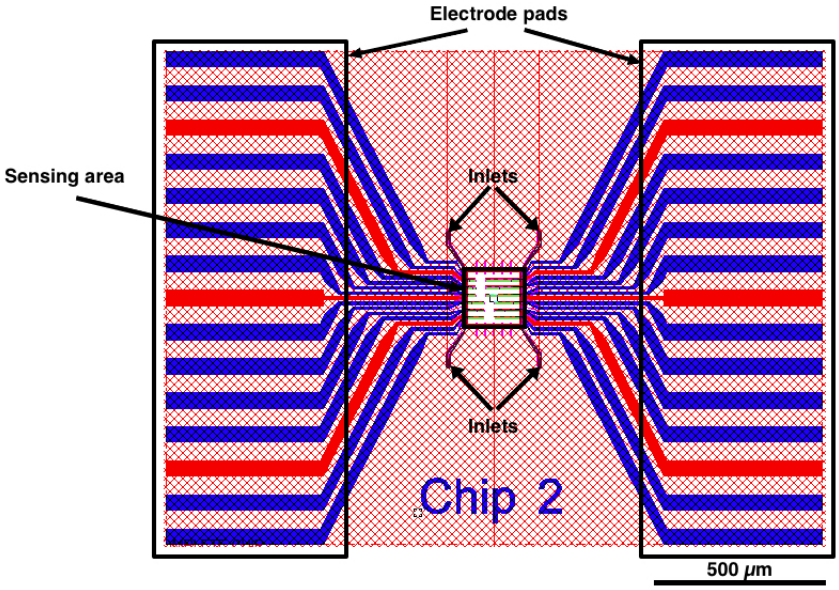
In this chapter, we report on the design of a microfluidic interface compatible with the fabricated SMRs chips.

4.1 Motivation

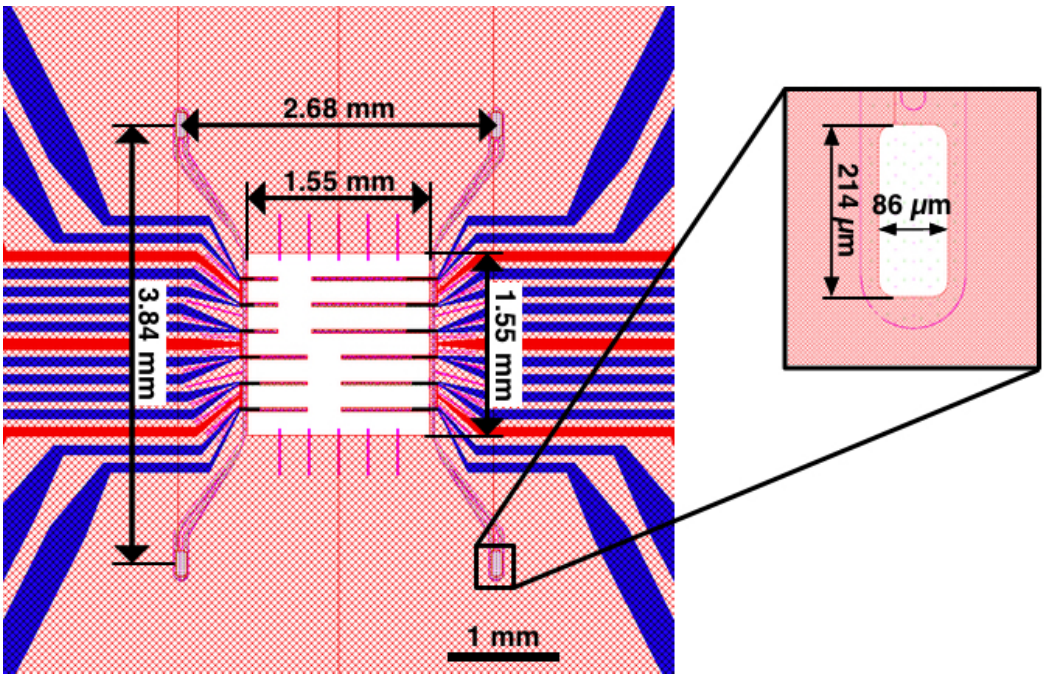
In addition to fabricating SMRs, the main objective of this project was to develop a microfluidic interface to characterize and test our devices. Throughout the semester, this was achieved in parallel to clean room work.
The interface requirements were considerable, but we highlight here the three highest priorities. First of all, the encapsulation should enable operation of the device both in air and in vacuum. Then, as the interface would carry fluids, optical transparency was desirable to efficiently monitor the experiments. Finally, easy reversibility of the interface assembly was crucial. If a single interface was being used and the chips could be quickly switched at the end of an experiment, costs would be greatly reduced.

4.2 Chip layout

Figure 60 depicts the CleWin layout of a chip made of cantilevers. On every chip of interest, the inlets and the sensing area were designed with the same dimensions and located at the same positions. The sensing area containing the resonators is a perfect square with sides of 1.55 mm, and the four microfluidic inlets, of dimensions 86 x 214 μm, are situated near the corners of this area, their centers separated by 2.68 mm and 3.84 mm. The lack of space between the sensing area, around which a vacuum chamber needs to be implemented, and the inlets, which have to be connected to microfluidic channels, was the main challenge that we faced for the realization of this interface.



(a) The electrodes pads lie on both sides of the chip, and the four inlets are located around a central sensing area containing the resonators.



(b) Closer view of the sensing area with the dimensions of interest. Inset : dimensions of the inlet openings.

Figure 60: CleWin layout of a chip with cantilevers. The dimensions shown are identical for all chips of interest.

4.3 Material

4.3.1 Early considerations

The first obvious candidate for the interface material was PDMS. Among other advantages, it is cheap, transparent and easy to process (see Section 2.4.1). If the devices did not need to be operated in vacuum, this material would be ideal, as it has been for many elementary microfluidic systems over the years.

A wafer-level packaging consisting of a pyrex capping bonded to the chip under vacuum conditions, as explored in [4], necessitates considerable time for processing the glass wafer. Additionally, as it would require clean room equipment, this solution is far from cost effective. We briefly considered machining a bulk glass. Nevertheless, due to its brittle nature, glass is very challenging to process. Special tools and expertise are thus needed, drastically increasing the costs.

4.3.2 3D-printing cured resin

The recent purchase of a stereolithography-based 3D-printer (*FormLabs*, Form 1+) by the LMIS1 laboratory prompted us to explore its capacities. Depending on the application, different resins, based on a mixture of methacrylic acid esters and photoinitiator, can be cured [25]. For evident reasons, we chose to use a transparent resin (Clear Resin GPCL02), which also turned out to exhibit the highest tensile strength at yield of all FormLabs resins. With the 3D-printer, we could develop numerous prototypes.
The main issue with this material is that no data could be found about the gas permeability of the cured resin. Hermeticity of a 3D-printed interface for operation in vacuum was thus studied (see Section 4.3.4).

4.3.3 PMMA

The material which we adopted for our final interface was poly (methyl methacrylate) (PMMA), better known under one of its trade name, *Plexiglas*. Low-cost and transpar-

ent, this thermoplastic is shatter-resistant and therefore often used as an alternative to glass [26]. Additionally, and in contrast with glass, it is easily machinable with conventional methods.

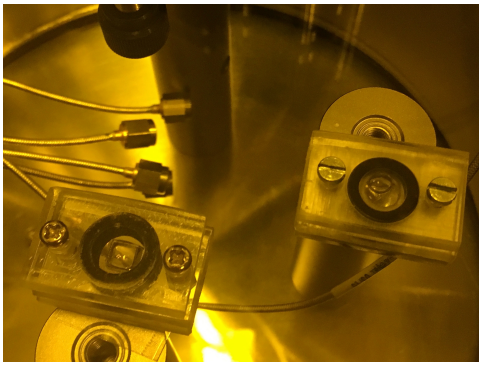
Due to the polymer nature of PMMA, its compatibility with vacuum applications was questioned. Tan et al. took advantage of its mechanical properties and claimed PMMA was impermeable to air [27]. They realized a peristaltic micropump based on PDMS-to-PMMA bonding, where the PMMA element was patterned into pneumatic chambers. Further experiments were conducted to study the permeability of PMMA in vacuum (see Section 4.3.4).

4.3.4 Vacuum experiments

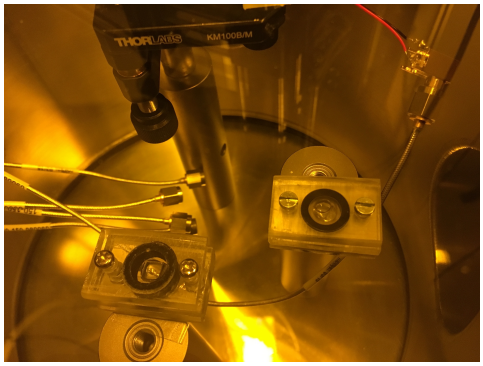
We conducted simple experiments to check the permeability of both 3D-printed material and PMMA. The first assembly was made of two 4 mm-thick PMMA elements encapsulating a droplet of water with an o-ring in between. The second assembly was made of two identical PMMA pieces sandwiching a 4 mm-thick 3D-printed element. This second device was also sealed with o-rings and again, a water droplet was placed in the center.

The PMMA elements were patterned with a CO_2 laser cutter (*Full Spectrum LASER*, H-Series 20x12), while the 3D-printed piece was realised by a Form 1+ printer from *FormLabs*.

The devices were placed in a vacuum chamber (Figure 61) connected to a vacuum pump (*Pfeiffer Hi Cube*). After 2 hours of experiment, the pressure had decreased down to 10^{-3} $mbar$ and the shape of the bubble inside the device was qualitatively studied. As can be seen in Figure 61, nothing seemed to have changed for either the PMMA device (on the right of the chamber) nor the sandwiched 3D-printed assembly (on the left). We therefore concluded that, at low levels of vacuum, the materials were not allowing gas and liquids to diffuse through.



(a) Situation at the beginning of the experiment (t=0, atmospheric pressure).



(b) Situation at the end of the experiment (t=120 minutes, $p = 10^{-3}$ mbar)

Figure 61: Experiment conducted for a qualitative study of the exchange of gas and liquids between the interior of sealed PMMA and 3D-printed devices and the environment. We could assess the impermeability of the PMMA and 3D-printed materials.

4.4 Sealing

Rather quickly, we focused on an assembly similar to what Khan developed in his doctoral thesis [12]. The main difference between Khan's devices and ours is the location of the fluidic inlets and outlets. Khan designed his inlets on the bottom side of the chip and could completely isolate the fluidic connections from the vacuum chamber (on top). In our case, the inlets are on the top side and must somehow coexist with the vacuum chamber encapsulating the sensing area.

4.4.1 First interface design

Our first interface idea consisted in developing a system that would be entirely placed in a vacuum chamber. Figure 62 depicts an exploded SolidWorks view of this solution. The sealing of the microfluidic channels would be achieved with o-rings. The PMMA connector would be compressed onto the chip by a steel element situated on top of the device and fixed with screws. Additionally, a vacuum-compatible epoxy glue should be used to hermetically seal the tubes to the connector. The tubes themselves should be made of suitable material, such as PEEK. Finally, an additional interface would be needed to get the fluidic connections

out of the vacuum chamber itself. Without even considering the electrical connections, this design appeared excessively difficult and was ruled out.

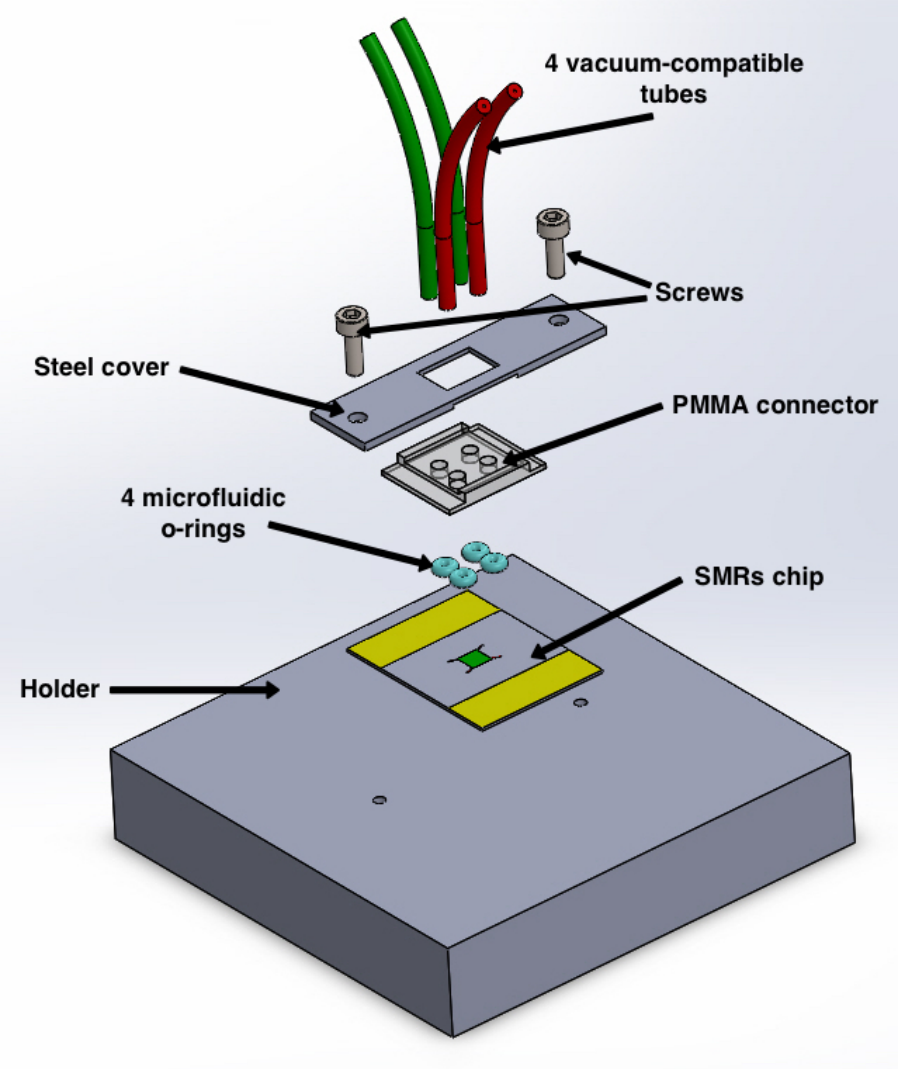


Figure 62: Exploded SolidWorks view of the first interface design thought. All the components used are described.

4.4.2 Second interface design

The interface that we developed recycled a concept already considered in the first design. Indeed, the connection to the inlets was achieved with o-rings. The main difference was that instead of having vacuum surrounding our complete device, we opted for the design of a small vacuum chamber enclosed in the connector. That chamber is sealed with a larger o-ring surrounding the inlets. The PMMA connector is pressed onto the o-rings by two screws located on the chip sides free of contact pads. On top of the PMMA piece, another vacuum o-ring and a glass lid are placed to ensure airtight sealing. Under the chip, a thin PDMS layer is placed to avoid direct contact of the chip back-side to the holder. Roughness of the holder could cause the chip to break when pressure is applied from the top. Our design is very similar to Khan's [12], but more challenging because the inlets are on the top-side. Figure 63 shows an exploded view of our solution, with the denomination of each element. The choice of o-rings is discussed in detail in Section 4.4.4.
Here, the electrical connections have not been pictured. Nevertheless, the PMMA connector covers only a limited part of the pads, making wire-bonding to a PCB possible.

4.4.3 Connector design

The PMMA element ensuring the "world-to-chip" connection was machined by the *Atelier de l'Institut de microtechnique (ATPR)*. Therefore, our design had to meet the requirements asked for standard machining.
The vacuum chamber was designed as a square with sides of 2.4 mm and round corners. As the window was machined with a drill, those round corners, with a radius of 0.5 mm, were unavoidable. A margin of about 400 μm was added on each side of the sensing area to minimize the risk of touching the devices with the connector, as well as account for the inevitable tolerances of machining.
The connector was further designed with five channels (four microfluidic "L-channels" and one straight vacuum channel). The microfluidic channels were defined with a diameter of 500 μm, matching the internal diameter of the commercial tubes connected to them (see Section 4.5).
O-ring grooves were designed following the reasoning of Section 4.4.4.

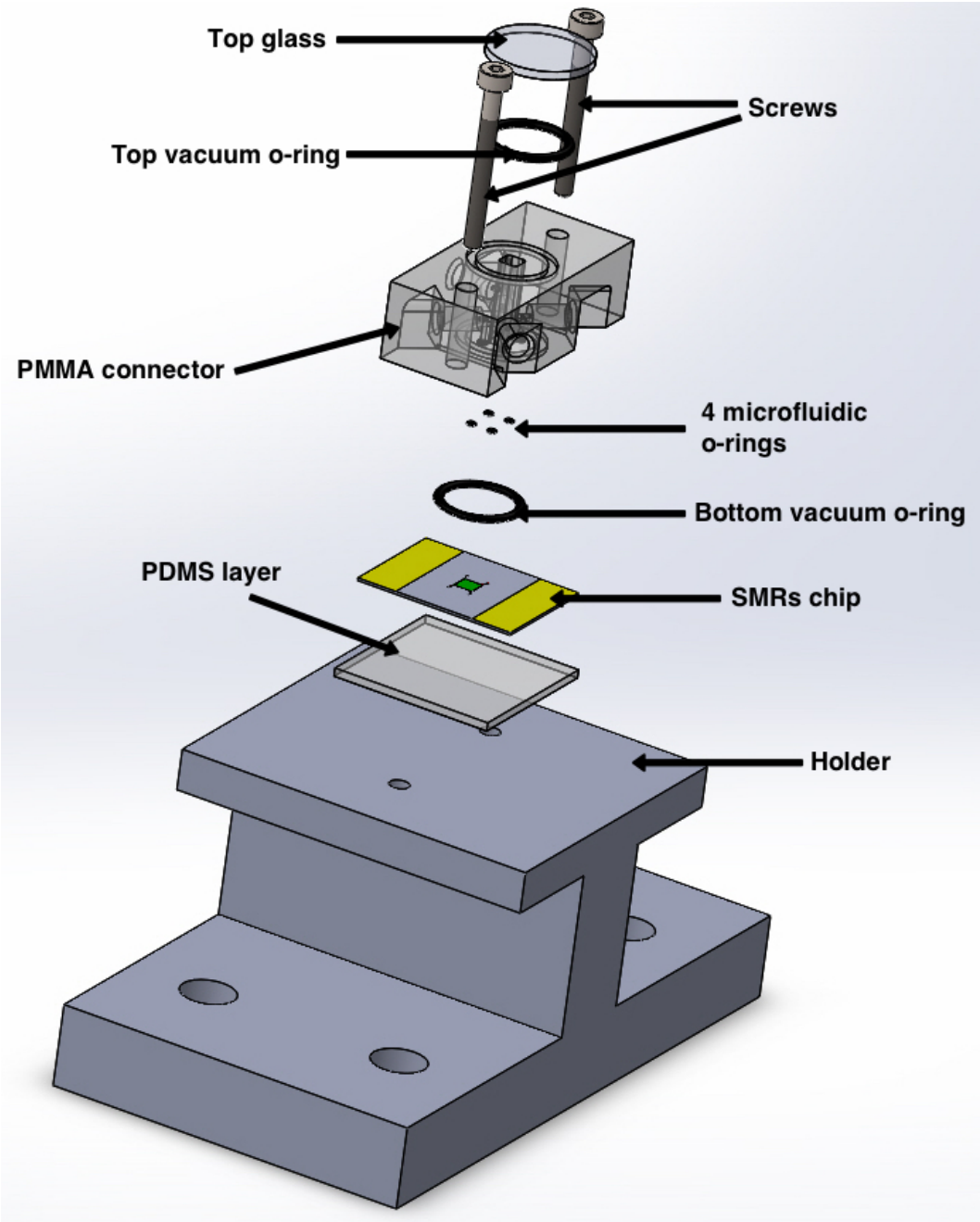


Figure 63: SolidWorks exploded view of the interface. All elements are denominated.

Finally, the thickness of the connector was reduced on the sides in order to avoid touching the chip in the case of a strong bending.

The drawing of the connector can be found in Appendix , and is pictured in Figure 64.

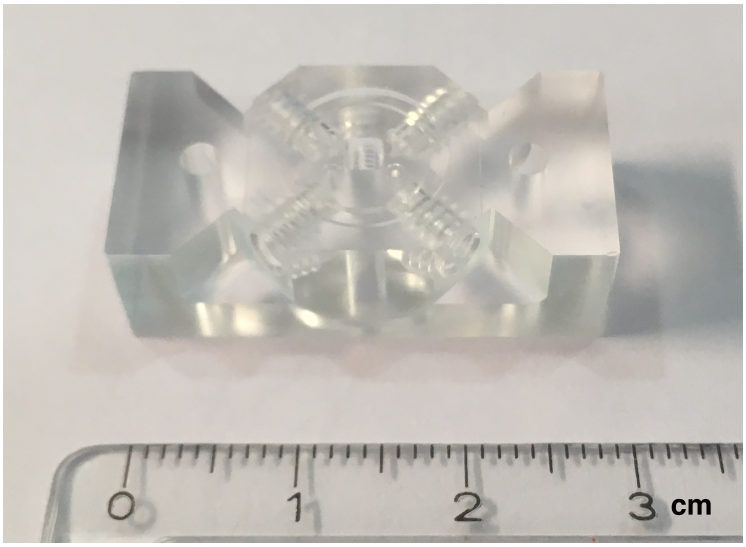


Figure 64: PMMA connector.

4.4.4 O-ring selection and grooves design

O-rings have proved to be convenient for vacuum sealing [12] and microfluidic connections [4]. In our interface, we are going to use them for both applications. The four small microfluidic o-rings connecting to the inlets of the chip have vacuum on their outside and will tend to expand, while the two vacuum o-rings sealing the chamber have vacuum on their inside and will tend to shrink. As such, all o-rings were considered to form vacuum sealings.

Angst + Pfister defined that all standard materials could be used as o-rings for normal vacuum operation (up to 10^{-5} $mbar$). For high-vacuum (between 10^{-6} and 10^{-9} $mbar$, only FPM (fluoroelastomer), CR (chloroprene elastomer) and FFKM (perfluoroelastomer) grades have proved suitable. In the ultra-high vacuum range, only FPM and FFKM should be used [28]. According to our experience, the *Pfeiffer Hi Cube* vacuum pump was reaching

vacuum levels as high as 10^{-4} $mbar$. For our application, we could thus use any o-ring material.

The four microfluidic o-rings ensured connection from 500 μm-diametral channels (see Section 4.4.3) to 86 x 214 μm rectangular inlets (see Section 4.2). To avoid fluid leakage, it was necessary to select o-rings having their lengths of seal larger than those features. The length of seal represents the cross-sectional dimension between the centers of the o-ring tores. It is equal to the sum of the inside diameter and the width of the o-ring (see Figure 65). In addition to that, the outside diameter of the microfluidic o-rings is limited by the lack of space arising from the large central window. Finally, the width of the o-ring needed to be sufficiently large so that the sealing area was significant.

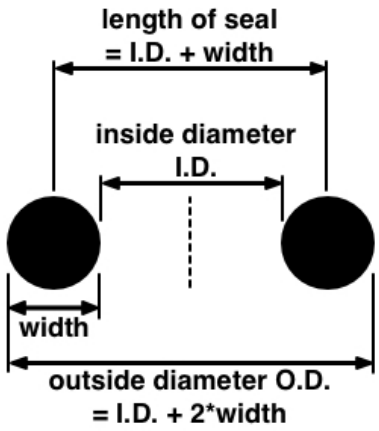


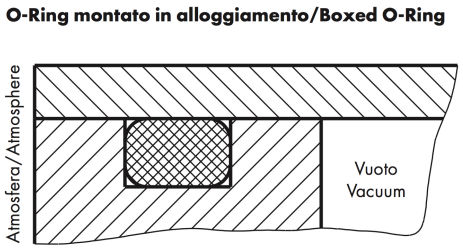
Figure 65: Cross-section schematics of an o-ring with a definition of its dimensions.

We contacted a few companies (*Apple Rubber*, *A. Aubry AG*, *ISOSWISS*) selling micro o-rings and obtained free samples. We settled for the NBR (Acrylonitrile butadiene elastomer) Shore 70 o-rings from *A. Aubry AG* having the following dimensions : $I.D. = 0.35$ mm and $w = 0.40$ mm. Those o-rings have a length of seal of 0.75 mm, well above the minimum required of 0.5 mm (corresponding to the diameter of the microfluidic channels in the connector). Additionally, accounting for the tolerances of the connector regarding the location of the grooves, it was ensured that the inlets would be completely enclosed.

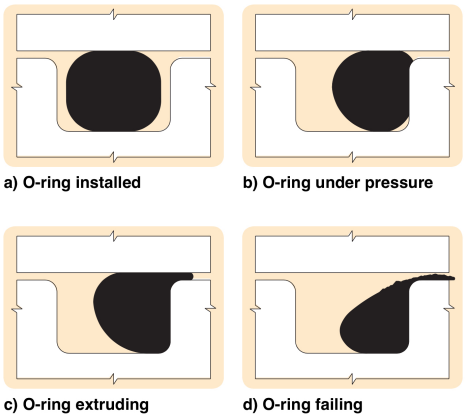
The inside diameter of the vacuum o-rings needed to be sufficiently large to enclose the four microfluidic o-rings. We settled for an inside diameter of 8 mm. The thickness of those o-rings was higher than the microfluidic o-rings, because we desired to have a larger sealing area with the chip. Indeed, the bottom vacuum o-ring is going to contact a very irregular surface because of the 6 μm-high poly-silicon islands defined (see Section 3.3). Enabling a larger area of contact thus increased the success rate of the vacuum sealing. We chose an o-ring width of 1 mm, because that configuration was also provided by *A. Aubry AG.*

The definition of o-ring grooves in the PMMA connector was required to contain and support the o-rings [29]. First, they serve alignment purposes. Without them, it would become extremely difficult to align and maintain in place five o-rings while fixing the connector. Additionally, when lower pressures are reached in the chamber, the atmospheric pressure exerts a high inward pressure on the vacuum o-rings. Similarly, when liquid is inserted in the channels, the microfluidic o-rings are going to feel an outward force. The presence of grooves thus avoids any undesirable shrinkage or expansion of our o-rings.

To ensure a functional o-ring vacuum sealing, a few guidelines must be followed [28]. First, it is important that the mounted o-ring fills the groove with a ratio between 90% and 100% (Figure 66a). Moreover, to avoid failure of the seal when subjected to a high pressure, it is required to minimize the opening through which the o-ring could extrude (see Figure 66b). Ideally, there would be no opening at all. In our case, it is not conceivable to have the connector touching the chip, because it would severely damage the electrodes and the channels, due to the scratching at the interface. Figure 67 indicated that we were far from risking extrusion. Indeed, the difference of pressure would be around 1 *bar* in our case (atmospheric pressure on one side, vacuum on the other), and our 0.1 mm gap lied well below the critical curve for a Shore hardness durometer of 70. The last significant condition to meet to have a good vacuum sealing is that the o-ring has to be squeezed by about 30%. This compression improves the area of contact and further increases the path of gas willing to leak.



(a) Ideal vacuum seal : the groove is filled to a ratio higher than 90% and the surfaces of the elements in contact [28].



(b) Example of o-ring failure due to extrusion. The distance between the two surfaces of the elements was too large to handle a higher pressure [29].

Figure 66: Schematics of a successful and failing o-ring vacuum seal.

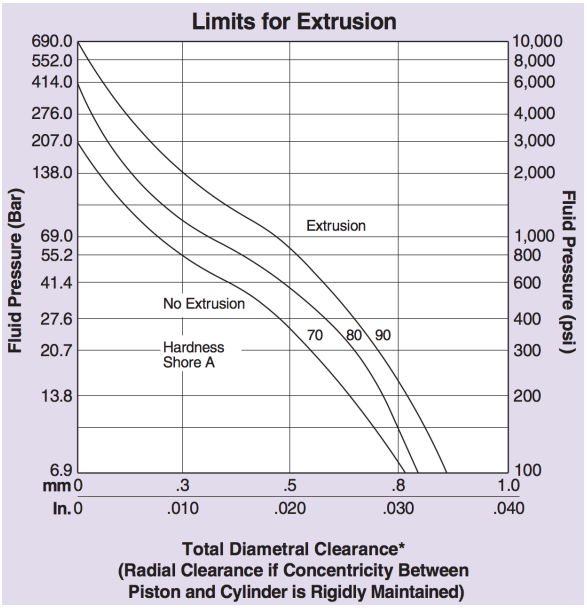


Figure 67: Maximum pressure supported with respect to the gap dimension to avoid extrusion of the o-ring. We notice that our case (1 bar pressure, 0.1 mm clearance) is well below the critical curve for a Shore hardness durometer of 70 [29].

Figure 68 shows a table extracted from [28], defining the grooves dimensions for vacuum applications implemented with o-rings widths ranging from 1.78 mm to 6.99 mm, which are the standard sizes available. Those dimensions ensure filling ratios of the grooves between 94 and 96%. As our o-rings have smaller widths, we performed a linear interpolation with MATLAB (see Figure 69) to compute the depth and width of the grooves needed. Table 8 summarizes the theoretical dimensions of our grooves following the interpolation.

Dimensioni della sede: **Groove dimensions:**
Sede retangolare, ricalcatura radiale **Rectangular groove, radial compression**

Diametro corda dell'O-Ring O-Ring cross-sectional diameter d_2	Profondità sede Depth of groove $D^{0}_{-0,05}$	Larghezza sede Width of groove $C^{\pm 0,05}$	Raggio Radius R_1	Raggio Radius R_2	Compressione O-Ring O-Ring compression	Grado di riempimento sede Filling ratio of groove
mm	mm	mm	mm	mm	%	%
1,78	1,25	2,10	0,10	0,25	29,7	95
2,0	1,40	2,15	0,10	0,25	30,0	95
2,5	1,75	2,65	0,10	0,25	30,0	95
2,62	1,85	3,10	0,10	0,25	29,4	94
3,0	2,10	3,20	0,10	0,25	30,0	95
3,5	2,45	3,70	0,10	0,25	30,0	95
3,53	2,50	4,15	0,10	0,25	29,2	94
4,0	2,80	4,25	0,20	0,50	30,0	95
5,0	3,50	5,30	0,20	0,50	30,0	95
5,34	3,70	6,30	0,20	0,50	30,7	96
6,99	4,90	8,20	0,20	0,50	29,9	95

Figure 68: Grooves dimensions for vacuum applications with standard o-rings widths [28].

The table from Figure 68 already considers that the o-rings are squeezed by 30% and that the surfaces are in contact, as depicted in Figure 66a. As it was already discussed, we are forced to leave a small gap between the connector and the chip. The depths of the grooves were therefore slightly reduced from their theoretical dimensions.

The gap between the connector and the chip was arbitrarily defined to 0.1 mm. The groove depth of the vacuum o-rings was thus reduced from 0.7 mm to 0.6 mm to maintain an axial compression of 30% on the o-ring. The microfluidic o-rings were subjected to a lower squeezing. We reduced their groove depth by only 80 μm, from 0.28 mm to 0.2 mm. The subsequent squeezing was measured to be

$$\text{Microfluidic o-ring squeezing} = \left|\frac{0.30 - 0.40}{0.40}\right| = 25\%$$

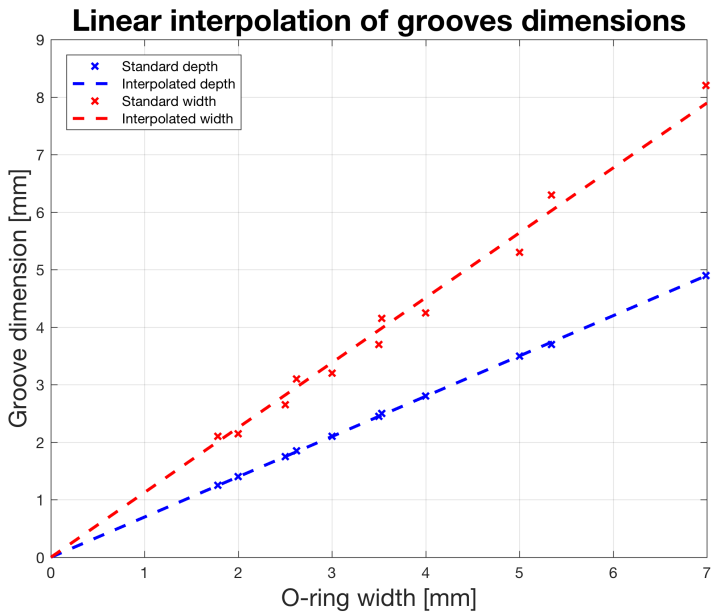


Figure 69: Linear interpolation of the depths and widths of grooves for vacuum applications.

Sealing type	**O-ring width**	**Groove depth**	**Groove width**
Microfluidic	0.4 mm	0.28 mm	0.42 mm
Vacuum	1 mm	0.7 mm	1.06 mm

Table 8: Dimensions of the grooves for microfluidic and vacuum o-rings.

The lower squeezing designed for the microfluidic o-rings allowed to reduce the pressure on the underlying microchannels. Since we restricted any radial expansion of those o-rings, the pressure was reported axially, acting directly on the channels.

Depending on the configuration of the system, an o-ring is slightly stretched or compressed when mounted. Positioned, the stretch or compression should never exceed 5% (2% are recommended) [29]. Since the vacuum o-rings were supported from their inside, their I.D. of 8 mm led to an groove diameter of 8.16 mm. The groove width was rounded to 1.1 mm. On the contrary, the microfluidic o-rings were supported from their outside. In this case, we chose not to subject those o-rings to anymore compression, and the grooves were designed

with the exact same diameter as the o-ring's O.D.

4.5 Fluidic connections

The connector was designed with 0.5 *mm*-diametral microfluidic channels sealed with o-rings (see Section 4.4). On the other side of the channels, the connector was designed for commercial fittings plugging. The smallest fittings that we found on the market are those offered by *IDEX Health & Science*. Their PEEK *Headless Super Flangeless Nuts* are designed with a US-standard 6-32 thread (in metrics, a nominal diameter of 3.50 *mm* with a pitch of 0.79 *mm*), and are compatible with tubings of 1/16" (1.59 *mm*) outside diameter. The complete integration works with corresponding ferrules that are surrounding the tubes and come into contact with the surfaces of interest, minimizing dead volume. An assembly of those elements, along with a cross section for higher clarity, are shown in Figure 70. To avoid any leakage, it is crucial that the tube be perfectly flat cut. Alternatively, it is conceivable to place the tubing slightly inside the ferrule, and only make the surface of the ferrule contact the PMMA connector. The drawback of this method is the apparition of a dead volume.

The same connection was planned for the vacuum connection to the pump. In that case, a flat surface contact between the elements is even more critical than for the fluidics.

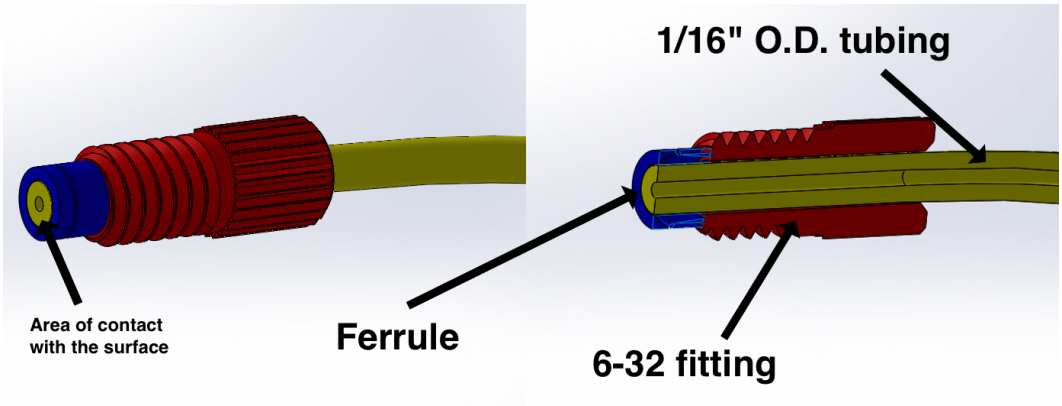


Figure 70: On the left, SolidWorks view of a fitting/ferrule/tubing assembly. On the right, corresponding cross-section.

4.6 Electrical connections

This aspect of the interface has been undertaken in another master project. Nothing is thus reported on this work.

4.7 Complete design

Figure 71 shows a SolidWorks view of the complete interface after assembly. Additionally to the elements already presented, an intermediate piece was designed to connect the *IDEX-HS* fitting to the standard KF25 ending of the *Pfeiffer Hi Cube* vacuum pump tubing. All four fluidic tubes could be mounted with fittings on both sides to facilitate connections to standard fluidic equipment such as a neMESYS syringe pump (*CETONI GmbH*).

The drawing of the KF25-connected piece can be found in Appendix .

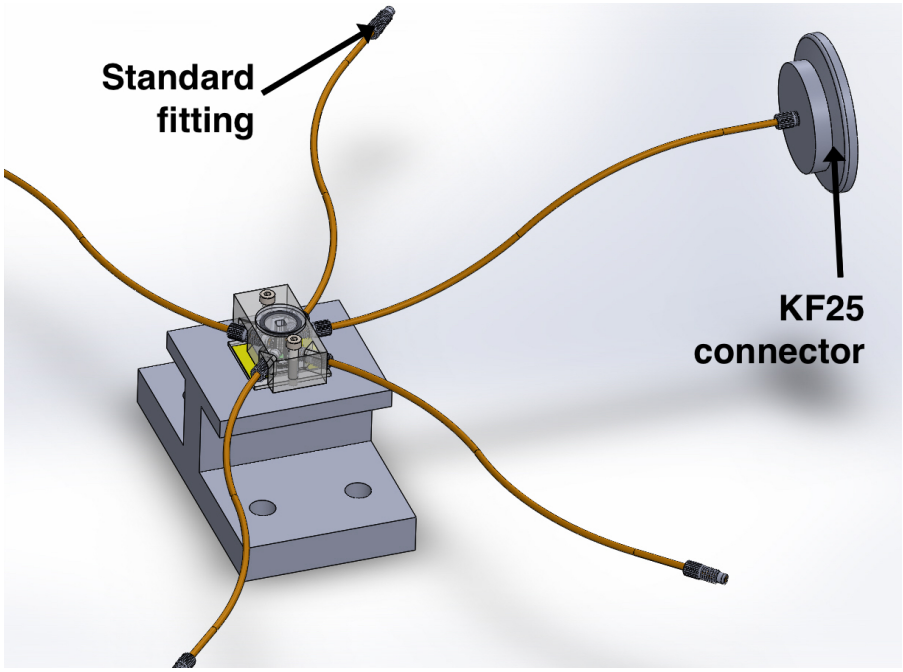


Figure 71: SolidWorks view of the complete interface after assembly. The KF25 connector can be joined to Pfeiffer Hi Cube vacuum pump tubing, while the fittings can be connected to standard fluidic equipment.

5 Simulations

In this chapter, we report on the simulations and calculations performed to ensure proper operating of the microfluidic interface.

5.1 Sealing force

As mentioned in Section 4.4.4, the o-rings need to be squeezed by about 30% to guarantee a successful vacuum sealing. In our interface, this compression force is achieved by the two screws fixing the connector into the holder.

Figure 72 shows a graph comprising extensive information on o-ring compression taken from the *Apple Rubber* Seal design guide [30]. The x-axis represents the percentage of compression (from 5% to 40%), while the y-axis is labelled "force applied per linear inch of seal in pounds". The length of seal of a simple o-ring is its "contact diameter" (see Section 4.4.4). This graph indicates the range of the force that must be applied in order to obtain a given compression, depending on the durometer and the cross-sectional width of the o-rings in inches. According to *Apple Rubber*, values for nonstandard cross-sections and omitted durometers can be inferred from a simple linear interpolation of the data available. Our o-rings have a Shore hardness durometer of 70 and cross-sections of 1 mm (for the vacuum o-rings) and 0.4 mm (for the microfluidic o-rings, see Section 4.4.4).

As Figure 72 shows ranges of values for each compression ratio, durometer and standard o-ring cross-section, we interpolated the required force for our smaller o-rings with both the average and the highest value extracted from the graph. Table 9 shows the data inferred for a 30% compression and a durometer of 70, for each of the cross-sections available. The conversion from the "force applied per linear inch of seal in pounds" unit to the "force applied per linear mm in Newtons" can be computed using the following relationship:

$$\frac{[N]}{[mm]} = \frac{[lb] \cdot 4.4482\ [N/lb]}{[in] \cdot 25.4\ [mm/in]}$$

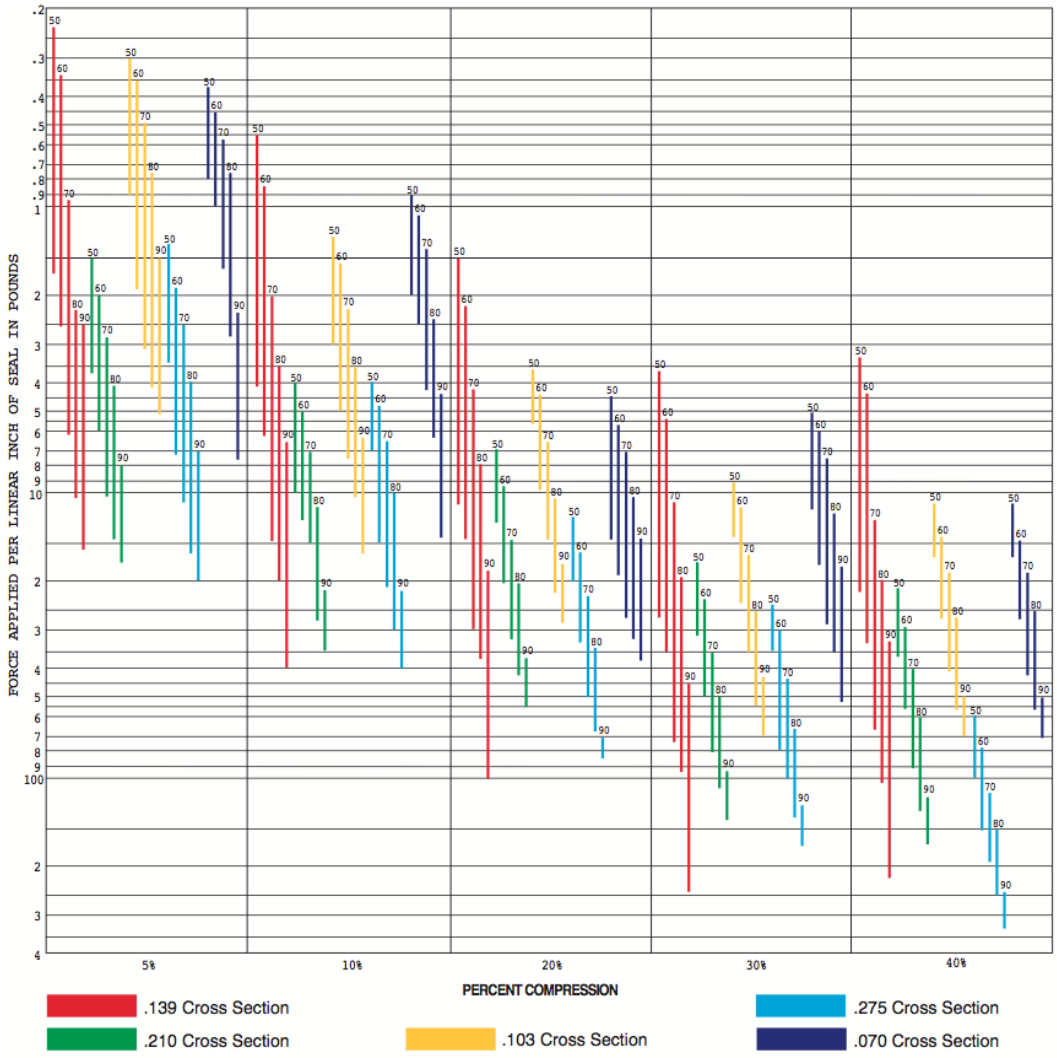


Figure 72: Force necessary to achieve given o-ring compression ratios for different durometers and cross-sections [30].

Figure 73 shows a linear interpolation of both the average and the highest force based on data from Table 9. We notice that the data set for the third largest cross-section is much higher than the interpolation line for both the highest and the average force. Having a closer look at Figure 72, we observed that the necessary force to apply to an o-ring of 0.139 *in* width was higher for a compression ratio of 30% than for 40%. As it was the only cross-section exhibiting such a behaviour, we decided to consider those values as outliners.

Cross-section [in]	0.07	0.103	0.139	0.210	0.275
Cross-section [mm]	1.778	2.616	3.531	5.334	6.985
Average force [lbs/ lin. in]	15	25	40	52.5	70
Average force [N/ lin. mm]	2.627	4.378	7.005	9.194	12.259
Highest force [lbs/ lin. in]	28	35	72	80	100
Highest force [N/ lin. mm]	4.904	6.129	12.609	14.010	17.513

Table 9: Average and highest forces necessary to achieve a 30% squeeze of o-rings of different cross-sections. Data extracted from Figure 72.

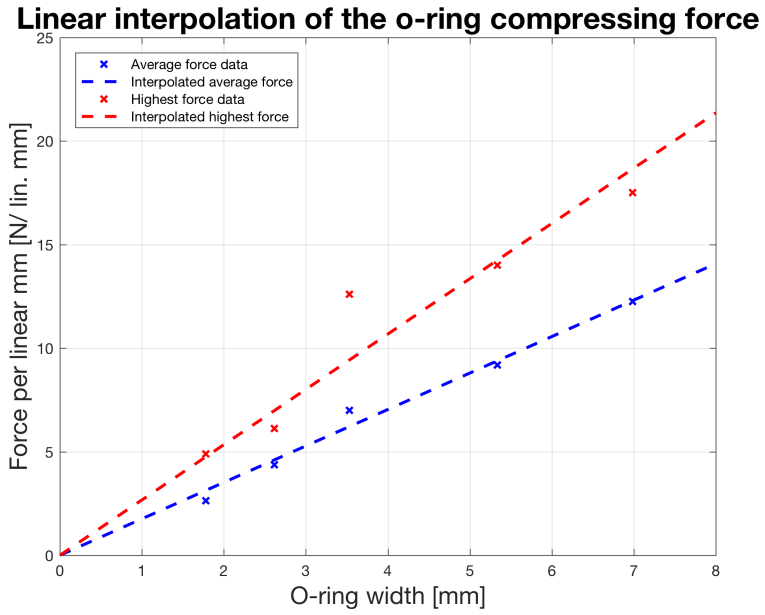


Figure 73: Linear interpolation of the force necessary to ensure a 30% squeeze with o-rings of durometer 70.

From the interpolation pictured in Figure 73, we obtained that for a 0.4 mm-cross-sectional o-ring, the highest necessary sealing force was 1.068 $N/\ lin.\ mm$ and the average force 0.704 $N/\ lin.\ mm$. The values for an o-ring of 1 mm width were 2.671 $N/\ lin.\ mm$ for the highest force and 1.760 $N/\ lin.\ mm$ for the average force.

The sealing length of a microfluidic o-ring was then calculated :

$$SL_{\mu\text{-fluidic o-ring}} = \pi \cdot (w_{\mu\text{-fluidic o-ring}} + I.D._{\mu\text{-fluidic o-ring}}) = \pi \cdot (0.4 + 0.35) = 2.356\ mm$$

Similarly, for the vacuum o-ring :

$$SL_{\text{vacuum o-ring}} = \pi \cdot (w_{\text{vacuum o-ring}} + I.D._{\text{vacuum o-ring}}) = \pi \cdot (1 + 8) = 28.274\ mm$$

Knowing the sealing length of our o-rings, we could compute the required force (average and highest) to achieve a 30% compression on each of them. For a microfluidic o-ring:

$$F_{max,\mu\text{-fluidic o-ring}} = 2.356\ mm\ \cdot\ 1.068\ N/\ lin.\ mm = 2.516\ N$$

$$F_{average,\mu\text{-fluidic o-ring}} = 2.356\ mm\ \cdot\ 0.704\ N/\ lin.\ mm = 1.659\ N$$

Similarly, for the vacuum o-ring :

$$F_{max,\text{vacuum o-ring}} = 28.274\ mm\ \cdot\ 2.671\ N/\ lin.\ mm = 75.520\ N$$

$$F_{average,\text{vacuum o-ring}} = 28.274\ mm\ \cdot\ 1.760\ N/\ lin.\ mm = 49.762\ N$$

The total forces to apply on the connector are then computable:

$$F_{max,tot} = 4\ \cdot\ F_{max,\mu\text{-fluidic o-ring}} + F_{max,\text{vacuum o-ring}} = 85.584\ N$$

$$F_{average,tot} = 4\ \cdot\ F_{average,\mu\text{-fluidic o-ring}} + F_{average,\text{vacuum o-ring}} = 56.398\ N$$

5.2 Connector bending

Knowing the theoretical force that is going to be applied on our o-rings, we were able to estimate if the bending of the connector following its fixation on the chip could become problematic.

We simulated the connector bending in COMSOL. Figure 74 describes the conditions applied in the simulation. The sealing forces calculated in Section 5.1 were applied on the two screws pushing the PMMA connector downwards. On the other side, the o-rings grooves were configured as fixed constraints.

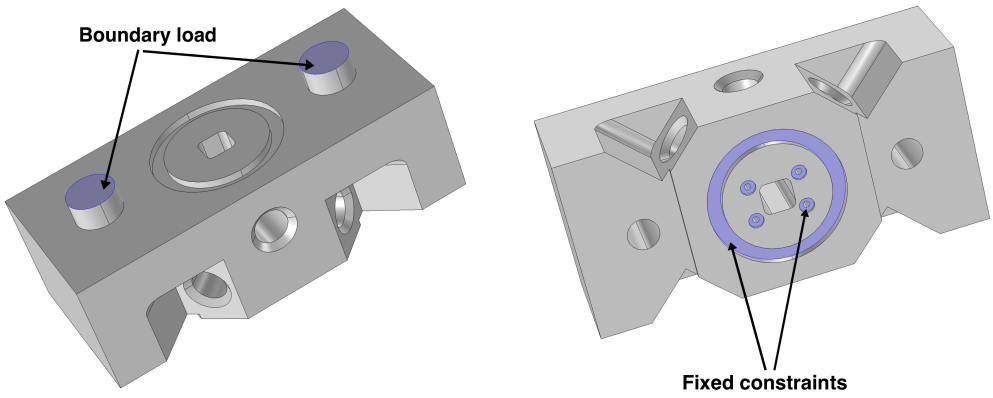
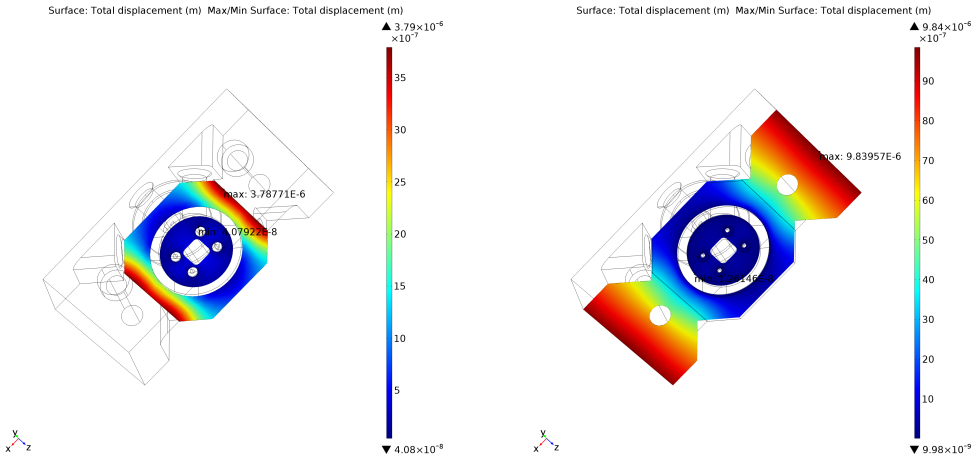


Figure 74: Conditions applied in the PMMA connector bending COMSOL simulation.

Figure 75 shows the results of the simulation with a boundary load of 85.584 N (highest theoretical force applied on the connector). We notice that the central area, designed to be separated by 100 μm from the chip, exhibited a maximum deformation of 3.788 μm. Additionally, the maximum deformation on the edges was 9.840 μm. Those results showed that the connector was not going to touch the chip at any point, and that its deformation would have little impact on the o-ring sealing.



(a) The highest displacement of the connector area closest to the chip was computed to be 3.788 μm. *This deformation leaves plenty of margin before potentially touching the chip.*

(b) The displacement of the edges of the connectors was also simulated and yielded a deformation in the range of 10 μm. *Again, it is largely acceptable.*

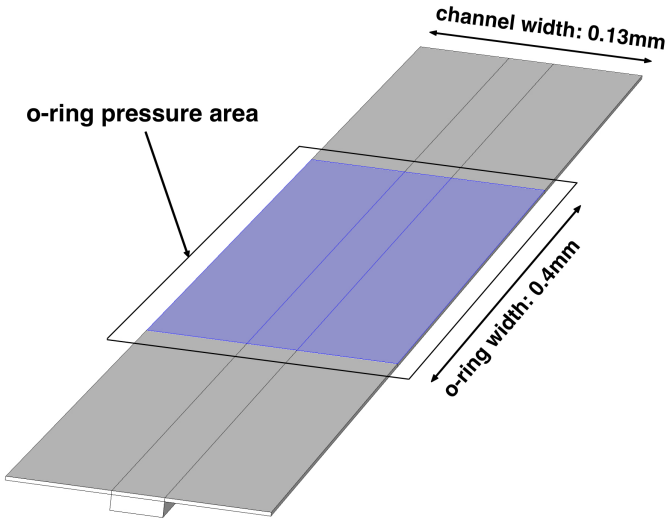
Figure 75: COMSOL simulation of the PMMA connector's bending.

5.3 Microchannels deformation

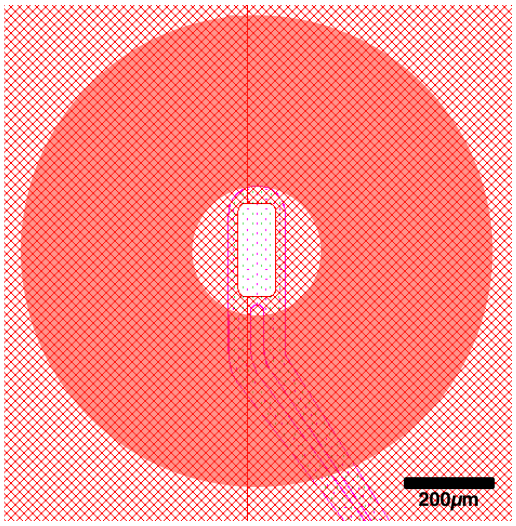
As the microfluidic o-rings are placed around the inlets, sections of the o-rings are required to lay on top of the microchannels. During the assembly, the connectors are pushed down, compressing the o-rings to ensure sealing. There is thus a real concern that the silicon nitride top layer of the channel may break if the force applied is too large.

This simulation comprised a section of the top layer of the channel alone (represented in Figure 76a). The sides of this element were fixed constraints, because they simulated the presence of the poly-silicon, considered here as not deformable. All other surfaces were allowed to deform vertically under the o-ring pressure, applied on the channel with its entire width of 0.4 mm. As a comparison, Figure 76b depicts the actual position of the o-ring on top of the channel as designed in CleWin.

We conducted the three simple simulations pictured in Figure 77. At first, the channel was considered without pillars nor central rigid element (a). Then, we added the central element



(a) Description of the simulation of the channel deformation. The blue area in the middle of the channel represents the region contacted by the o-ring. All the sides are constrained, while the remaining surfaces are free to bend.



(b) CleWin visualisation of the o-ring position on top of the channel.

Figure 76: Comparison of the o-ring superposition of the channel between the COMSOL simulation and the CleWin design.

(a) Simulation without pillars nor rigid central element. The entire layer is free to bend.

(b) Simulation without pillars but with the rigid central element, restricting any bending in the middle of the channel.

(c) Simulation with pillars and the rigid central element. It is the closest to the reality.

Figure 77: Backside view of the successive simulations conducted to estimate the bending of the channels. The coloured elements are rigid and reduce the layer deformation.

(b), and finally the pillars, designing a simulation as close as possible to the reality (c).

The deformations simulated for the top layer of silicon nitride are summarized in Table 10. We understood that in the absence of any additional rigid component in the channel, the top layer would collapse (deformation of 9.25 μm through a 6 μm-high channel). Adding the central part and the pillars to the simulation yielded much more acceptable results. In the closest case to the actual situation, the maximum deformation of 0.462 μm represented a reduction of the channel height by less than 10%. It was thus concluded that o-ring sealing would not have a significant impact on the flow inside the microchannels. Figure 78 shows a simulation of the deformation of a channel with the pillars and the central element.

Simulation #	**Max. deformation [μm]**
Simulation a	9.25
Simulation b	2.25
Simulation c	0.462

Table 10: Maximum deformation of the channel silicon nitride top layer under o-ring pressure for the three simulations conducted.

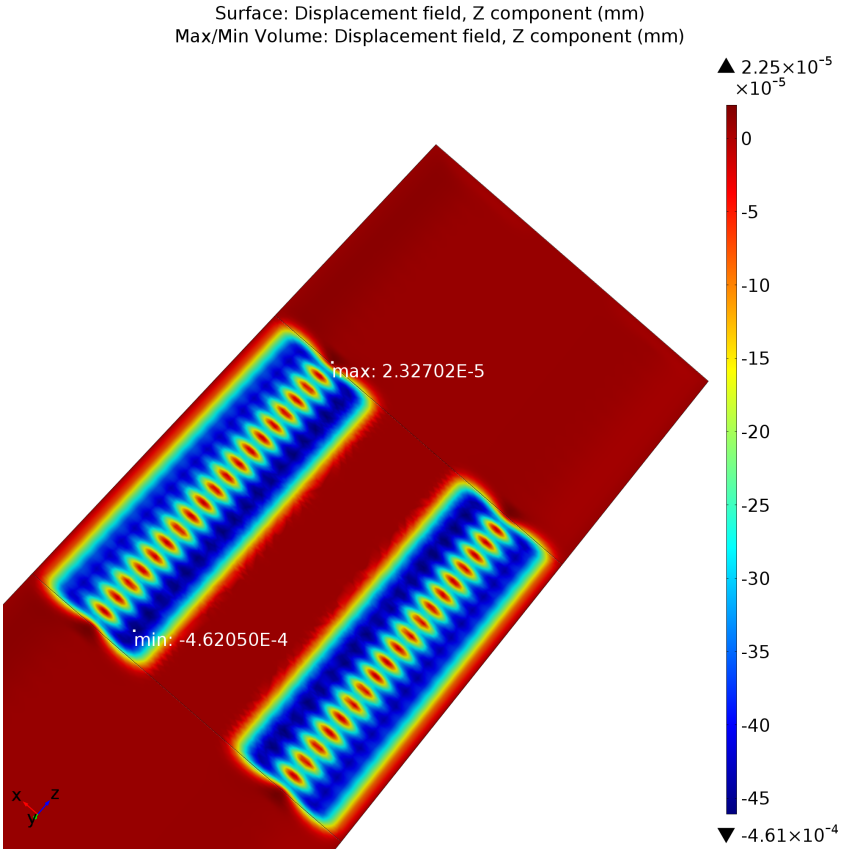


Figure 78: Most realistic simulation of the deformation of the channels. We observe that the maximum deformation is 0.462 μm.

6 Experimental results

In this section, we present the experiments conducted with a 3D-printed connector, along with the conclusions drawn from the results.

A few interfaces were created with the Form 1+ 3D-printer. Those pieces were very similar to the connector designed in Section 4.4.3. The main difference lied in the definition of the microfluidic channels. Printing pieces with different features sizes, we discovered that the minimum achievable channel diameter was 0.9 mm. Therefore, we did not even considered designing the vertical 500 μm holes, and focused only on printing horizontal channels. As 0.9 mm-diametral features were not reproducible, we decided for safety to go for diameters of 2 mm. The L-shaped fluidic path was then completed by manually drilling the vertical holes through the grooves. Figure 79 shows the back surface of the 3D-printed piece exhibiting the manually drilled holes in the centers of the grooves.

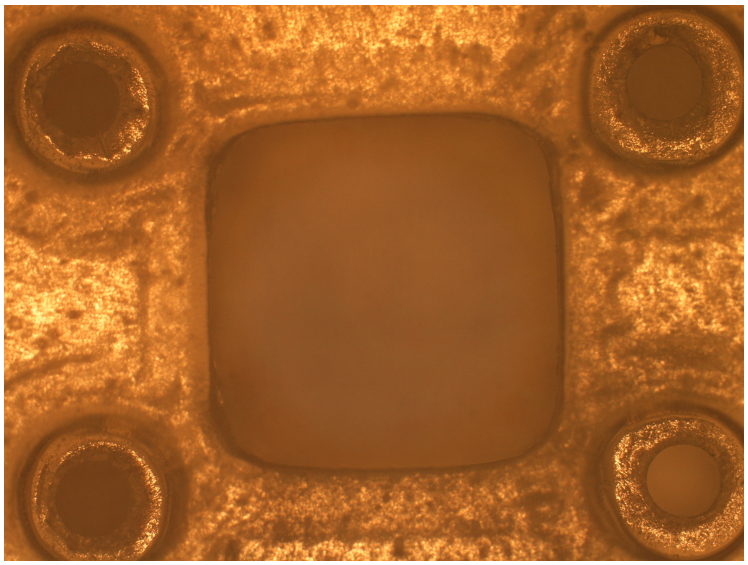


Figure 79: Back surface of the 3D-printed interface used for our experiments. The holes located in the center of the grooves were manually drilled.

6.1 PMMA sealing

For assessment of its functionality, the 3D-printed connector was assembled to a simple PMMA lid with microfluidic and vacuum o-rings (as in Figure 80). The PMMA piece was patterned with a CO_2 laser cutter (*Full Spectrum LASER*, H-Series 20x12). In addition to two through-holes designed for screwing the assembly, four small 0.5 μm-diametral holes were cut at the locations the inlets would occupy on a chip. Unfortunately, as can be observed in Figure 79, the surface of the 3D-printed piece exhibited some roughness. This impacted the quality of the grooves, causing difficulties to place and hold the o-rings during the assembly to the PMMA lid. Nevertheless, we succeeded in aligning the four microfluidic channels of the connector with the PMMA holes.

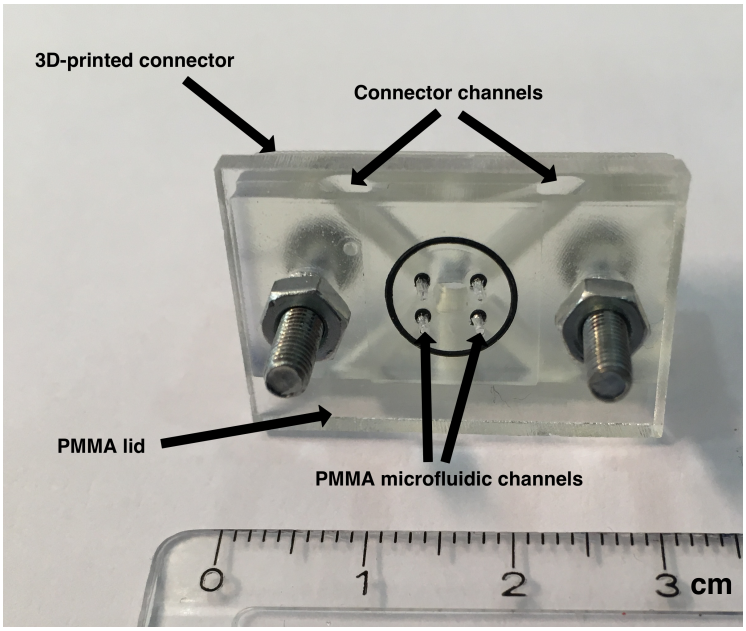


Figure 80: Assembly of a 3D-printed connector with a simple PMMA lid, in which holes were cut at the locations the inlets would occupy on a chip. We see here the four microfluidic o-rings enclosed by a larger o-ring.

Four tubes were then glued into the connector's channels. Wax was heated and applied around the tubes. After cooling down, it offered a reversible sealing for low pressure applications.

We then proceeded to send liquid through the channels. Black food colouring was mixed with water to enable better observation of the liquid flow, as well as potential leakage points. A syringe was then filled with the coloured water and installed on the unit of a *CETONI neMESYS* syringe pump. Figure 81 shows the complete experimental setup. Additionally to the *neMESYS* pump, a microscope was available to record experiments.

Sending liquid into the device at a flow of 500 $\mu l/min$, we did not notice any leakage point. The water was spilled from the PMMA hole corresponding to the connector channel in which the liquid was introduced. We could thus deduce that the o-ring seal was working properly. Increasing the flow to 1000 $\mu l/min$, we remarked that liquid started to fill a supposedly isolated channel (see Figure 82). We could not assess with certainty the origin of the leakage. It is conceivable that the liquid went through the connector. As it was manually drilled, the connector could have been internally damaged. Another possible, but less likely explanation, is that the microfluidic o-rings of both channels failed. Nevertheless, we could still conclude that the o-rings enabled operation up to a flow of 500 $\mu l/min$.

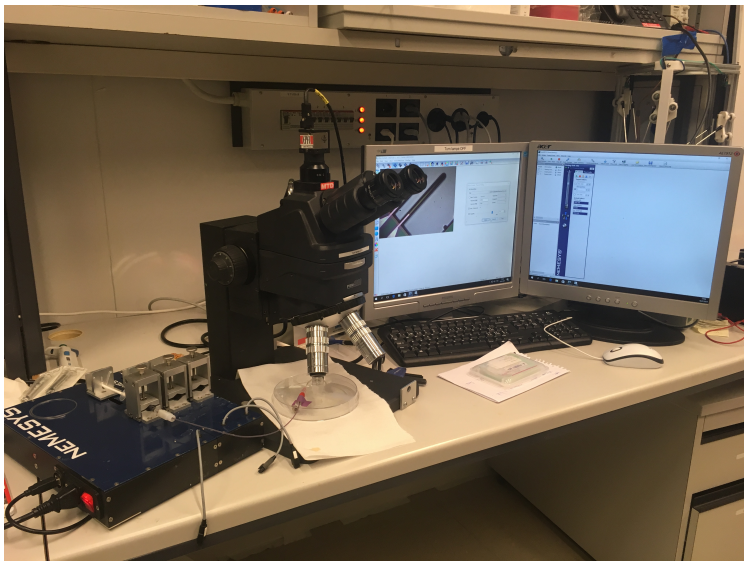


Figure 81: Overview of the neMESYS setup in LMIS4. A microscope is also available to record experiments.

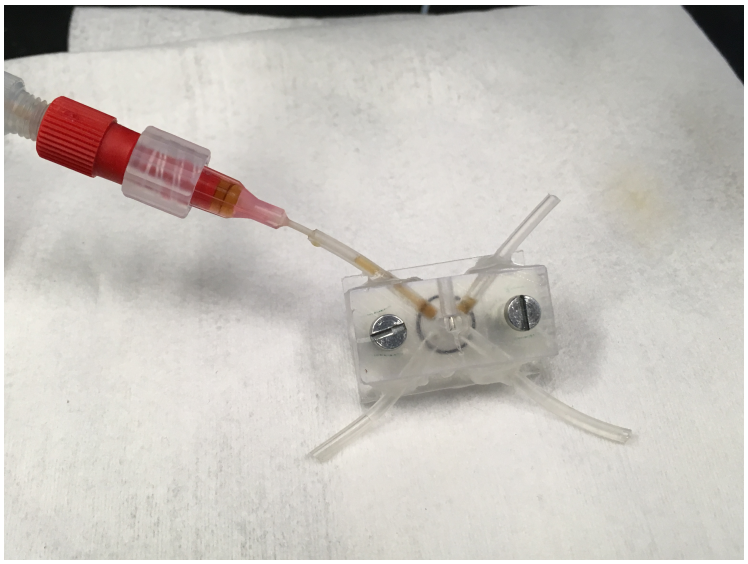


Figure 82: Device failing with a flow of 1000 $\mu l/min$ *(the channel on the right should not contain liquid). We could not determine whether the o-rings were leaking or if the liquid went through the connector.*

6.2 Chip sealing

An experiment was also attempted using an actual SMRs chip. Assembling the 3D-printed connector onto the chip turned out to be extremely challenging. We first tried to place the o-rings in the connector grooves. Since the roughness of the 3D-printing material did not offer flat and precise grooves, we did not succeed to maintain the o-rings in the connector as we tried to place it face down onto the chip. Therefore, we decided to place the o-rings directly on the chip, ensuring that they enclosed the inlets by monitoring the process at the microscope (Figure 83). The chip was then placed on the PMMA lid. The lid itself was inserted with screws such that they would be head down during assembly. The connector was then inserted around the screws and pushed onto the grooves. The assembly could finally be screwed together with nuts. Unfortunately, this method could not ensure alignment between the o-rings and the grooves. Additionally, the screwing process applied momentums on the o-rings. Possibly, the o-rings were moved with respect to their initial position.

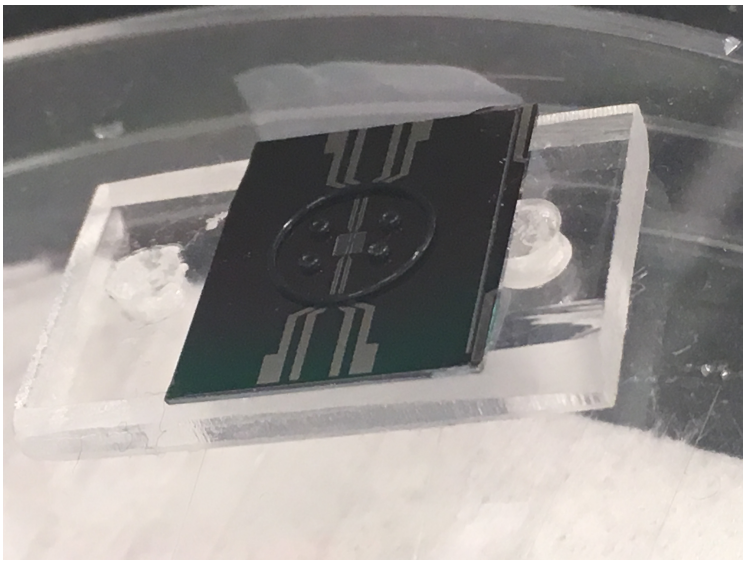


Figure 83: O-rings placed on top of the chip and aligned with the inlets before assembly.

We decided to send flow to the device anyway (Figure 84). Setting it to a very low value of 5 $\mu l/min$ to avoid high pressures in the microchannels, we noticed that the water never reached the microchannels. Instead, it started to leak from the wax seal. Our first assumption was that the pressure the liquid had to overcome to enter the microchannels was significantly higher than the wax seal strength. It is also conceivable that the o-rings were misaligned with the inlets and that we were pushing liquid against the close surface of the chip. On a brighter note, we observed that the o-ring did not break the microchannels. The silicon nitride layer seemed undamaged.

Even if the experiments with a 3D-printed connector reached little success, we are confident regarding the future developments of the project. Indeed, using a PMMA connector machined by the mechanical workshop's experienced people should yield much better results. First, the grooves are of higher quality from dimensional and surface roughness standpoints. For this reason, it is hoped that they could hold the o-rings during the assembly process. Then, the transparency of PMMA is definitely going to help with the alignment of the o-rings with the inlets. Finally, the commercial fluidic fittings, implemented with their ferrules, are expected to forbid any leakage.

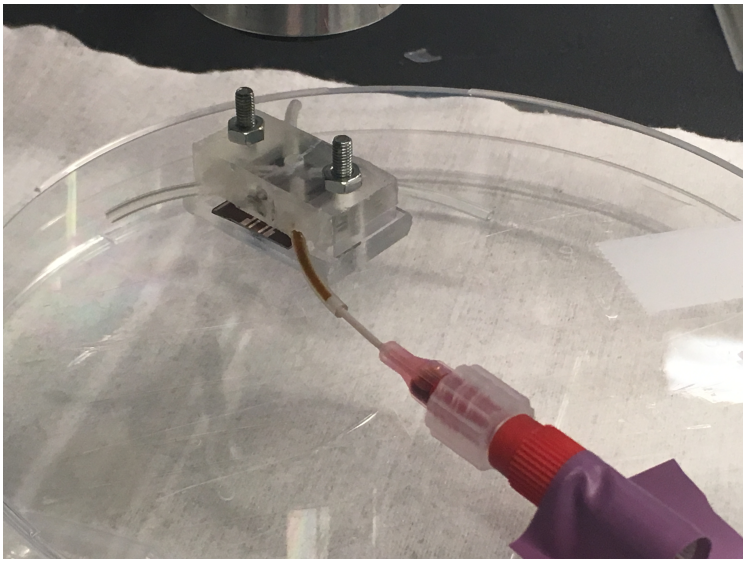


Figure 84: Assembled device connected to a syringe for fluid delivery.

7 Conclusion

In this project, numerous aspects of the field of microfluidic devices were explored. An important amount of time was dedicated to finish the fabrication of suspended microchannel resonators in the clean room. In parallel, an interface for those devices was developed from scratch. As the microfluidic platform had to meet many requirements (operation in vacuum, transparency, reversibility), a literature review was conducted to find the most suitable material and the most convenient sealing method.

After opting for PMMA and an o-ring-based sealing technique, connector prototypes were created with the help of 3D-printing. The final version of the connector was machined by the mechanical workshop. As apprehension arised regarding the bending of the connector and the deformation of the microchannels under the o-rings pressure, COMSOL was used to theoretically simulate the potential failure points of the assembly. Finally, some experiments were conducted with a 3D-printed prototype connector, which was assembled with o-rings. Sending fluids through our device, we could assess the microfluidic o-ring seals up to a flow of 500 $\mu l/min$.

This project marks great advances towards characterizing and testing SMRs in a reproducible manner. The future work to be achieved is to assemble the SMRs chips with the PMMA connector. Being transparent and exhibiting much nicer surface conditions, confidence is high that it will achieve higher performances than the 3D-printed prototype. Additionally, devices will have to be wire bonded to PCBs for actuation and detection purposes. Finally, the chips will be able to be tested in different environments (air or vacuum) and compared.

8 References

[1] Peter Enoksson, Göran Stemme, and Erik Stemme. Fluid density sensor based on resonance vibration. *Sensors and Actuators A: Physical*, 47(1):327 – 331, 1995.

[2] T. P. Burg and S. R. Manalis. Suspended microchannel resonators for biomolecular detection. *Applied Physics Letters*, 83(13):2698–2700, 2003.

[3] Christiane Ziegler. Cantilever-based biosensors. *Analytical and Bioanalytical Chemistry*, 379(7):946–959, 2004.

[4] T. P. Burg, A. R. Mirza, N. Milovic, C. H. Tsau, G. A. Popescu, J. S. Foster, and S. R. Manalis. Vacuum-packaged suspended microchannel resonant mass sensor for biomolecular detection. *Journal of Microelectromechanical Systems*, 15(6):1466–1476, Dec 2006.

[5] Thomas P. Burg, Michel Godin, Scott M. Knudsen, Wenjiang Shen, Greg Carlson, John S. Foster, Ken Babcock, and Scott R. Manalis. Weighing of biomolecules, single cells and single nanoparticles in fluid. *Nature*, 446(7139):1066–1069, 04 2007.

[6] Robert A. Barton, B. Ilic, Scott S. Verbridge, Benjamin R. Cipriany, Jeevak M. Parpia, and Harold G. Craighead. Fabrication of a nanomechanical mass sensor containing a nanofluidic channel. *Nano Letters*, 10(6):2058–2063, 2010. PMID: 20443578.

[7] J. Lee, R. Chunara, W. Shen, K. Payer, K. Babcock, T. P. Burg, and S. R. Manalis. Suspended microchannel resonators with piezoresistive sensors. *Lab Chip*, 11:645–651, 2011.

[8] Gabriel Vidal-Álvarez, Eloi Marigó, Francesc Torres, and Núria Barniol. Fabrication and measurement of a suspended nanochannel microbridge resonator monolithically integrated with cmos readout circuitry. *Micromachines*, 7(3):40, 2016.

[9] Yuksel Temiz, Robert D. Lovchik, Govind V. Kaigala, and Emmanuel Delamarche. Lab-on-a-chip devices: How to close and plug the lab? *Microelectronic Engineering*, 132:156 – 175, 2015. Micro and Nanofabrication Breakthroughs for Electronics, {MEMS} and Life Sciences.

[10] Mark A Eddings and Bruce K Gale. A pdms-based gas permeation pump for on-chip fluid handling in microfluidic devices. *Journal of Micromechanics and Microengineering*, 16(11):2396, 2006.

[11] Thierry Corman, Peter Enoksson, Kjell Norén, and Göran Stemme. A low-pressure encapsulated resonant fluid density sensor with feedback control electronics. *Measurement Science and Technology*, 11(3):205, 2000.

[12] M. Faheem Khan. *Microchannel resonators to characterize liquid samples*. PhD thesis, Department of Micro and Nanotechnology - Technical University of Denmark, 2012.

[13] Ata Tuna Ciftlik and Martin A. M. Gijs. Parylene to silicon nitride bonding for post-integration of high pressure microfluidics to cmos devices. *Lab Chip*, 12:396–400, 2012.

[14] Anthony K. Au, Wonjae Lee, and Albert Folch. Mail-order microfluidics: evaluation of stereolithography for the production of microfluidic devices. *Lab Chip*, 14:1294–1301, 2014.

[15] C. W. Hull. *US Pat.* 06/638905, 1986.

[16] Sidra Waheed, Joan M. Cabot, Niall P. Macdonald, Trevor Lewis, Rosanne M. Guijt, Brett Paull, and Michael C. Breadmore. 3d printed microfluidic devices: enablers and barriers. *Lab Chip*, 16:1993–2013, 2016.

[17] S. Takenaga, B. Schneider, E. Erbay, M. Biselli, Th. Schnitzler, M. J. Schöning, and T. Wagner. Fabrication of biocompatible lab-on-chip devices for biomedical applications by means of a 3d-printing process. *physica status solidi (a)*, 212(6):1347–1352, 2015.

[18] Andrew M Christensen, David A Chang-Yen, and Bruce K Gale. Characterization of interconnects used in pdms microfluidic systems. *Journal of Micromechanics and Microengineering*, 15(5):928, 2005.

[19] Gerardo Perozziello, Frederik Bundgaard, and Oliver Geschke. Fluidic interconnections for microfluidic systems: A new integrated fluidic interconnection allowing plug'n'play functionality. *Sensors and Actuators B: Chemical*, 130(2):947 – 953, 2008.

[20] D Snakenborg, G Perozziello, O Geschke, and J P Kutter. A fast and reliable way to establish fluidic connections to planar microchips. *Journal of Micromechanics and Microengineering*, 17(1):98, 2007.

[21] Ana C. Glavan, Ramses V. Martinez, E. Jane Maxwell, Anand Bala Subramaniam, Rui M. D. Nunes, Siowling Soh, and George M. Whitesides. Rapid fabrication of pressure-driven open-channel microfluidic devices in omniphobic rf paper. *Lab Chip*, 13:2922–2930, 2013.

[22] Jung Jin Park, Xiaolong Luo, Hyunmin Yi, Theresa M. Valentine, Gregory F. Payne, William E. Bentley, Reza Ghodssi, and Gary W. Rubloff. Chitosan-mediated in situ biomolecule assembly in completely packaged microfluidic devices. *Lab Chip*, 6:1315–1321, 2006.

[23] CMi SPIDER 600. https://cmi.epfl.ch/thinfilms/Spider600.php, Consulted on Jan 7, 2017.

[24] Gerhard Franz, Robert Kachel, and Stefan Sotier. Residual free reactive ion etching of the bell contact ti/pt/au. *Materials Science in Semiconductor Processing*, 5(1):45 – 50, 2002.

[25] FormLabs. Clear photoreactive resin : Safety Data Sheet. https://formlabs.com/media/upload/Clear-SDS_u324bsC.pdf, Consulted on Jan 12, 2017.

[26] Poly(methyl methacrylate) — Wikipedia, The Free Encyclopedia. https://en.wikipedia.org/w/index.php?title=Poly(methyl_methacrylate)&oldid=759075499, Consulted on Jan 12, 2017.

[27] Hsih Yin Tan, Weng Keong Loke, and Nam-Trung Nguyen. A reliable method for bonding polydimethylsiloxane (pdms) to polymethylmethacrylate (pmma) and its application in micropumps. *Sensors and Actuators B: Chemical*, 151(1):133 – 139, 2010.

[28] Angst + Pfister. Angst + Pfister : O-ring basic catalogue. http://www.angst-pfister.com/en/dynasite.cfm?dsmid=120603, Consulted on Jan 12, 2017.

[29] Parker. Parker O-Ring Handbook. https://www.parker.com/literature/ORD%205700%20Parker_O-Ring_Handbook.pdf, Consulted on Jan 15, 2017.

[30] Apple Rubber. Apple Rubber : Seal design guide. http://www.applerubber.com/src/pdf/seal-design-guide.pdf, Consulted on Jan 12, 2017.

Appendices

Chip numbering

On the wafers, the chips were numbered as pictured in Figure 85, starting on the first row. Additionally, in each chip the inlets were also denominated.

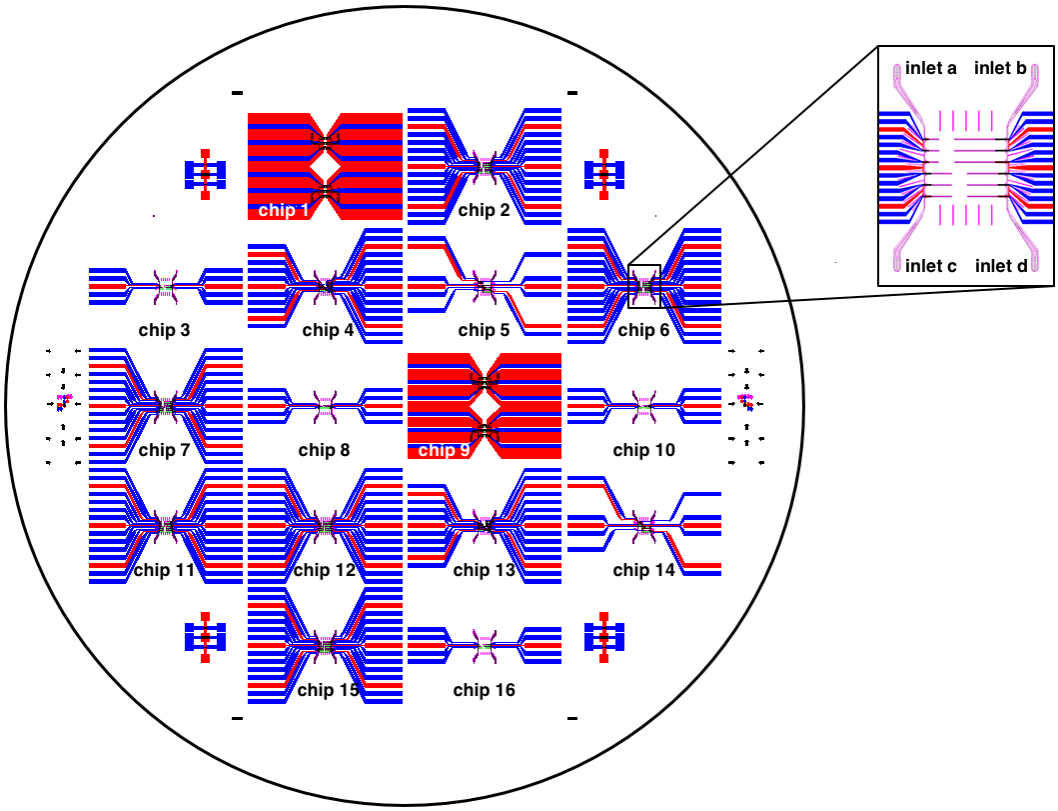
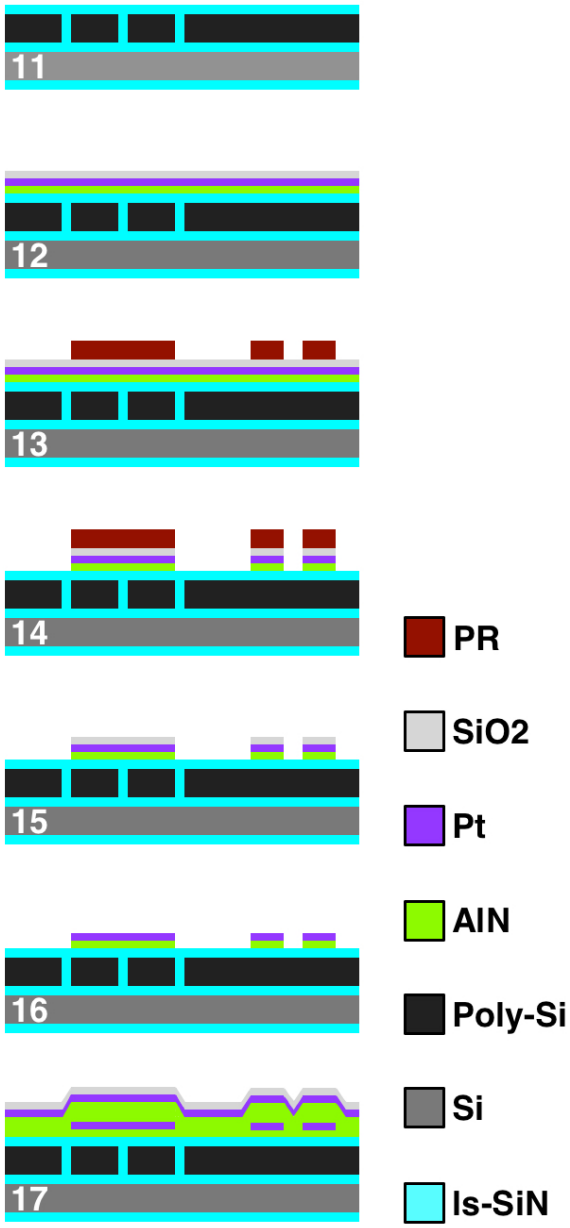
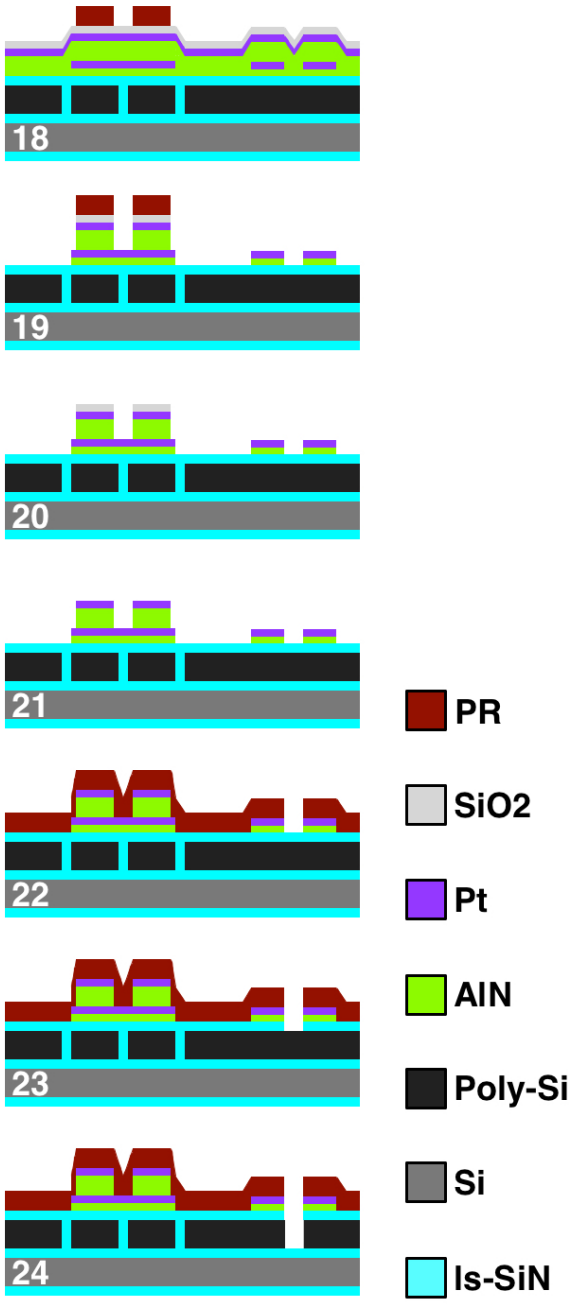


Figure 85: Chips and inlets denomination.

Process flow




18
19
20
21
22
23
24
PR
SiO2
Pt
AlN
Poly-Si
Si
ls-SiN

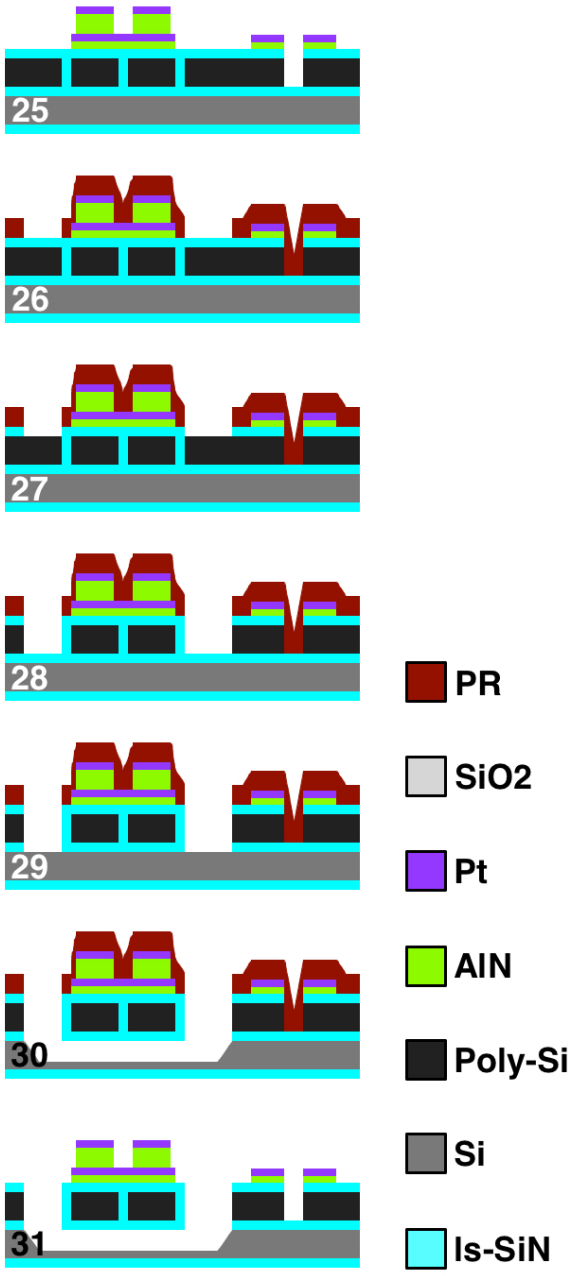


Figure 86: Process flow : the step number corresponds to the run-card.

Step N°	Description	Equipement	Program / Parameters	Target	Actual	Remarks
12	**ALUMINUM NITRIDE/PLATINUM SPUTTER DEPOSITION**					
12.1	Aluminum_Deposition	Z4/ Spider600	15 nm AlN (19" deposition)	DR: 50 nm/min, T=300°C, 40sccm N2/10sccm Ar, 1500 W plasma, 6W setpoint		Put a dummy wafer per each material, check that reflected power for dummy AlN is 0 over a 5' test deposition!
12.2	Platinum_Deposition	Z4/Spider600	25 nm Pt (6" deposition)	DR= 270nm/min, T=300°C, 1000 W plasma		Use the program AlN_T_D_Pt_T_D_**Etch**
12.3	Silicon Oxide_Deposition	Z4/Spider600	20 nm SiO2 (1' deposition)	DR= 20nm/min, T=room T, 1000 W		Use the program SiO2_F. Protective layer to prevent contact (and resisues) between PR and Pt. This deposition rate is highly unstable. Put a Silicon test wafer and check the oxide thickness after 1'. Then proceed with the deposition on real wafers according to the result.
12.4	Condictivity check	Multimeter	Check that R= OL			Check the deposition of the oxide
12.5	Inspection	Z6/uScope				
13	**PHOTOLITHOGRAPHY- Mask 3_Bottom_Contact**					
13.1	Dehydratation	Z1/Yes III HMDS	30' @ 125°C			
13.2	AZ ECI coating EBR PR Bake	Z1/Rite_track or ACS	C_AZ_ECI_2um or ACS program 0326 (HMDS included)	2 um		CD= 5 um (markers). EBR
13.3	PR exposure	Z5/MLA150	180 mJ/cm^2, defocus -3		MLA, 150 mJ/cm^2	Alignment. Marker 1-3: (-42274.63, 1250), (42274.63, 1250) (channels-bottom)
13.4	PR development PR PostBake	Z1/Rite_track or ACS	Dev_AZ_ECI_2um or program 0926			
13.5	Inspection	Z6/uScope	Resolution and alignment			
14	**OXIDE/ALUMINUM NITRIDE/PLATINUM DRY ETCHING**					

14.1	Silicon Oxide/Aluminum Nitride/Platinum Dry Etching	Z2/ STS Multiplex ICP	AlN_etch, around 55".	70 nm. Help yourself with end point detection. Start with 50'' and then proceed with 10'' steps. From when I see the peak of the Pt I should wait 50".	Wafer 7672 : 50" Wafer 7674 : 74"	$ER_{\_Pt}$=about 25 nm/min. $ER_{\_AlN}$=about 250 nm/min. $ER_{\_SiO2}$=about 70 nm/min. ETCHING ARTES CAN BE VERY UNSTABLE. I am not using IBE because of Pt redeposition, causing short circuits all over the wafer. The etching of the three materials is done with one program. Check that the wafer is not vibrating during the etching, otherwise we get burned PR and uncontrollable etching rate!
14.2	Contacts isolation check	Multimeter				
15	**PR_STRIP**					
15.1	Plasma O2 clean	Z2/Tepla	Strip_High , 5 min			
15.2	Remover 1165	Z2/WB_PR_Strip	Bath 1 : main remover	5min, 70°C		
15.3	Remover 1165	Z2/WB_PR_Strip	Bain 2 : clean remover	5min, 70°C		
15.4	Gentle rinse (bath 4)	Z2/WB_PR_Strip	DI Rinse (bath 4)	x 3 times		Avoid the fast rinsing to not break the microchannels
15.5	IPA Rinse	Z14/Solvent wet bench	IPA bath for 1 min			
15.6	Gentle Drying	Z2/WB_PR_Strip	10' laminar flow			Dry with N2 gun only the wafer backside. Avoid any direct flux on top of microchannels.
16	**SILICON OXIDE STRIP**					
16.1	SiO2 wet etching	Z14/Acid wet bench	BHF 7:1, 1 min	20nm SiO2		
16.2	Gentle rinse	Z14/Acid wet bench	DI Rinse x3			Avoid the fast rinsing to not break the microchannels
16.3	IPA Rinse	Z14/Solvent wet bench	IPA bath for 1 min			
16.4	Gentle drying	Z14/Solvent wet bench	Drying under laminar flow (about 5')			Dry with N2 gun only the wafer backside. Avoid any direct flux on top of microchannels.
16.5	Conductivity check	Multimeter	Check resistance of bottom pads	R=about 10 ohm		
16.6	Inspection	Z6/uScope				
16.7	Profile check	Z4/ Dektak		Check for fences and their height.		Fences, if there, should be as short as possible. High trenches could cause short circuit after the top contact deposition.
16.8	Inspection	Z6/SEM				Check fences.
17	**ALUMINUM NITRIDE/PLATINUM SPUTTER DEPOSITION**					

17.1	Aluminum_Deposition	Z4/ Spider600	300 nm (6' deposition)	DR: 50 nm/min, T=300°C, 40sccmN2/10sccm Ar, 1500 W plasma, 6W setpoint		DR=50nm/min
17.2	Platinum_Deposition		25 nm (6" deposition)	DR= 270nm/min, T=300°C, 1000 W plasma		DR=270nm/min
17.3	Silicon Oxide_Deposition	Z4/Spider600	20 nm SiO2 (1' deposition)	DR= around 20nm/min (UNSTABLE!!), T=room T, 1000 W		Use the program SiO2_F. Protective layer to prevent contact (and resisues) between PR and Pt. This deposition rate is highly unstable. Put a Silicon test wafer and check the oxide thickness after 1'. Then proceed with the deposition on real wafers according to the result.
18	**PHOTOLITHOGRAPHY- Mask 4_Top_Contact**					
18.1	Dehydratation	Z1/Yes III HMDS	30' @ 125°C			DO HDMS! Otherwise no PR adhesion on SiN.
18.2	AZ ECI coating EBR PR Bake	Z1/Rite_track or ACS	C_AZ_ECI_2um or ACS program 0326 (HMDS included)	2 um		CD= 2 um. EBR
18.3	PR exposure	Z5/MLA150	180 mJ/cm^2, defocus -3		150mJ/cm^2 defocus -3, MLA	Alignment. Marker 3-4.
18.4	PR development PR PostBake	Z1/Rite_track or ACS	Dev_AZ_ECI_2um or program 0926			
18.5	Inspection	Z6/uScope	Resolution and alignment			
19	**OXIDE/ALUMINUM NITRIDE/PLATINUM DRY ETCHING**					
19.1	Silicon Oxide/Aluminum Nitride/Platinum Dry Etching	Z2/ STS Multiplex ICP	AlN_etch (about 2'15")	20 nm SiO2+ 300 nm AlN + 25 nm Pt. Help yourself with end point detection. Start with 2' and then proceed with 10" steps.	Wafer 7672 : 122" Wafer 7674 : 110"	ER_Pt=about 25 nm/min. ER_AlN=about 250 nm/min. ER_SiO2=about 20 nm/min. ETCHING ARTES CAN BE VERY UNSTABLE. Start with 2' and proceed in steps. Wafer exchange: wait for the machine to load the wafer before starting the new process, otherwise "gate error"). Check EPD: when we are in the AlN we see a sinusoidal-like shape.

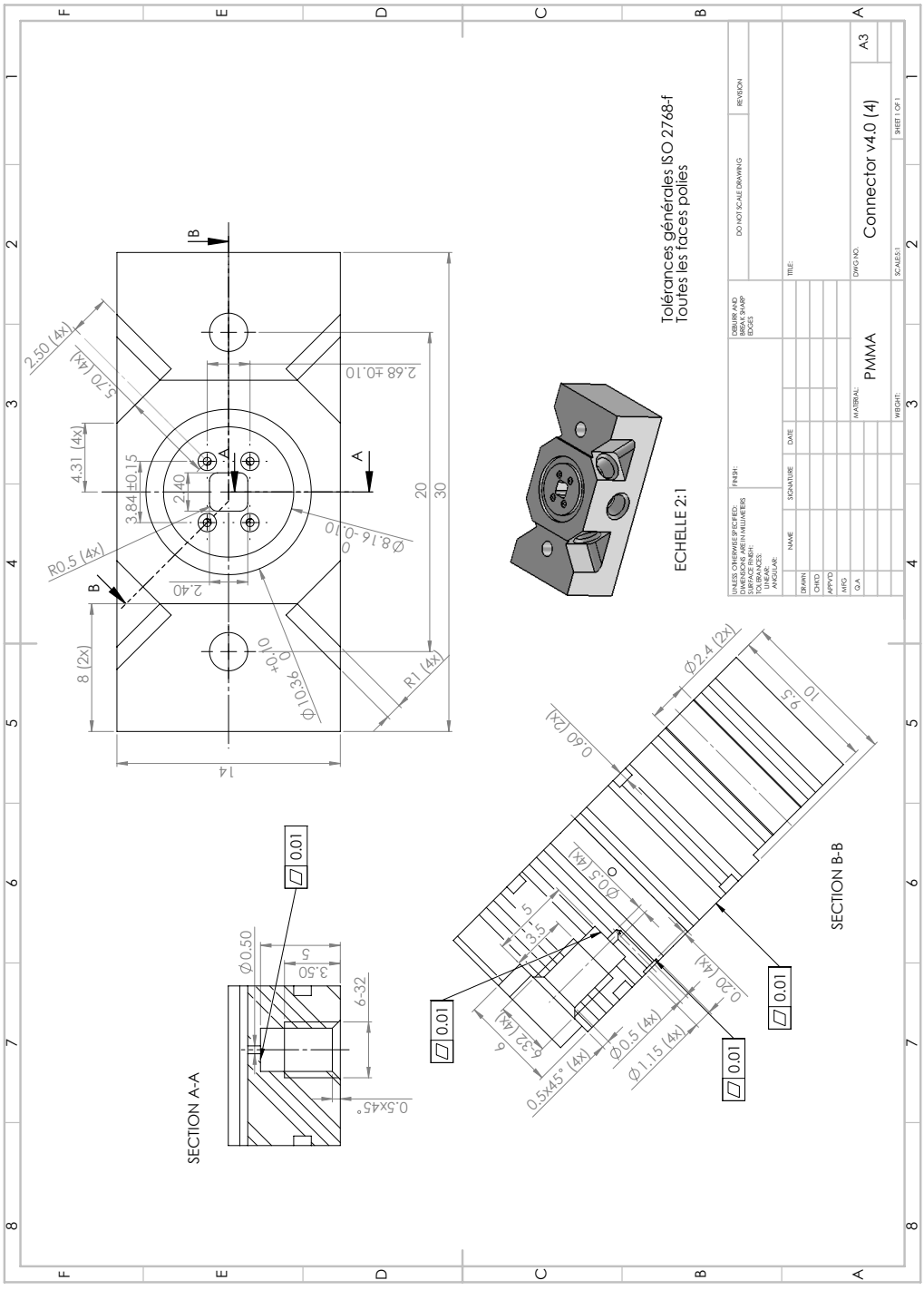
19.2	Inspection	Z6/uScope	Resolution and alignment			
19.3	Contact isolation check	Multimeter				
20	**PR_STRIP+CLEANING**					Necessary! Otherwise contamination/saturation of KOH
20.1	Plasma O2 clean	Z2/Tepla	Strip_High , 5 min			
20.2	Remover 1165	Z2/WB_PR_Strip	Bath 1 : main remover	5min, 70°C		
20.3	Remover 1165	Z2/WB_PR_Strip	Bain 2 : clean remover	5min, 70°C		
20.4	Gentle rinse (bath 4)	Z2/WB_PR_Strip	DI Rinse (bath 4)	x 3 times		Avoid the fast rinsing to not break the microchannels
20.5	IPA Rinse	Z2/WB_PR_Strip	IPA bath for 1 min			
20.6	Gentle Drying	Z2/WB_PR_Strip	10' laminar flow			Dry with N2 gun only the wafer backside. Avoid any direct flux on top of microchannels.
20.7	Inspection	Z6/uScope				
21	**SILICON OXIDE STRIP**					
21.1	SiO2 wet etching	Z14/Acid wet bench	BHF 7:1, 1 min	20nm SiO2		
21.2	Gentle rinse	Z14/Acid wet bench	DI Rinse x3			Avoid the fast rinsing to not break the microchannels
21.3	IPA Rinse	Z14/Solvent wet bench	IPA bath for 1 min			
21.4	Gentle drying	Z14/Solvent wet bench	Drying under laminar flow (about 5')			Dry with N2 gun only the wafer backside. Avoid any direct flux on top of microchannels.
21.5	Quick Conductivity check	Multimeter	Check resistance of bottom pads	R=about 10 ohm		Check if the etching reached the bottom pads.
21.6	Inspection	Z6/uScope				Check alignment and dimensions.
21.7	Conductivity check	Z16/PM8	Check isolation between bottom and top contacts (R>MΩ). Check also isolation between different bottoms.	R=about 10 ohm		To check: BC'-BC', BC'-BC'', TC'-TC', TC'-TC'', BC'-TC'.
21.8	Profile check	Z4/ Dektak		Check for fences and their height.		
21.9	Inspection	Z6/SEM	No tilt for dimension check. Tilt 45° to check the step.			Check how the step looks like (top contact going on top of the bottom contact)
22	**PHOTOLITHOGRAPHY-Mask 5_PolyIslands**					
22.1	HDMS	Z1/Yes III HMDS	30' @ 125°C			DO HDMS! Otherwise no PR adhesion on SiN.

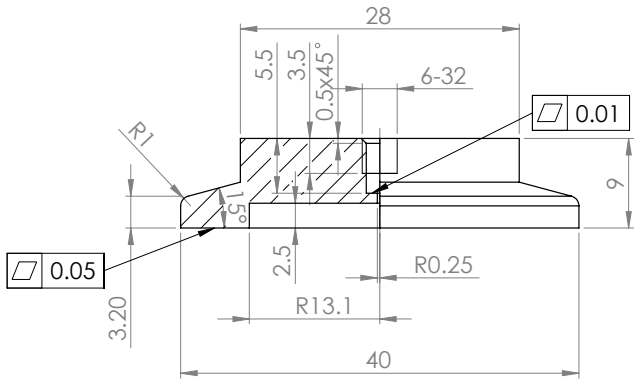
22.2	AZ ECI coating EBR PR Bake	Z1/Rite_track or ACS	C_AZ_ECI_5um or ACS program 0329 (HMDS included)	5 um	3 um coating	CD= 5 um (markers). EBR
22.3	PR exposure	Z6/MA6 (or MLA)	xxx s, Soft Contact (or MLA: 220mJ/cm^2, -3, high quality)		MLA, 180 mJ/cm^2	Alignment. Marker 3-5.
22.4	PR development PR PostBake	Z1/Rite_track or ACS	Dev_AZ_ECI_5um or ACS program 0929		3 um developed	
22.5	Inspection	Z6/uScope	Resolution and alignment			
23	**LOW STRESS SILICON NITRIDE DRY ETCHING**					
23.1	Silicon Nitride Dry Etch	Z2/ A601E	Nitrure_1: 5'	depends on wafer, check		ER_SiNx=300nm/min ER_{PR}=300nm/min
23.2	Inspection	Z6/uScope	Resolution and alignment			See the change in color, Polysilicon is greyish
24	**POLYSILICON DRY ETCHING**					
24.1	PolySilicon Dry Etch	Z2/ A601E	ANISO_ADP: 1'31"	6 um		ER_{PR}=130nm/min
24.2	Inspection	Z6/uScope				Do NOT etch bottom SiN!
24.3	Etching check	Z3/Nanospec	Check Si+Is-SiN thickness	500 nm (between the electrical tracks)		
24.4	Profile check	Z4/Dektak		etching depth/wall profile		
25	**PR_STRIP+CLEANING**					
25.1	Plasma O2 clean	Z2/Tepla	Strip_High , 5 min			
25.2	Remover 1165	Z2/WB_PR_Strip	Bath 1 : main remover	5min, 70°C	15min	3x5'
25.3	Remover 1165	Z2/WB_PR_Strip	Bain 2 : clean remover	5min, 70°C	15min	3x5'
25.4	Gentle rinse (bath 4)	Z2/WB_PR_Strip	DI Rinse (bath 4)	x 3 times		Avoid the fast rinsing to not break the microchannels
25.5	Gentle Drying	Z2/WB_PR_Strip	10' laminar flow			Dry with N2 gun only the wafer backside. Avoid any direct flux on top of microchannels.
25.6	Plasma O2 clean	Z2/Tepla	Strip_low , 3 min			
25.7	Inspection	Z6/uScope				
25.8	Conductivity check	Z16/PM8	Check isolation between bottom and top contacts (R>MΩ). Check also isolation between different bottoms.	R=about 10 ohm on the same pad. R=Mohm betwenn dfferent tracks, and top/bottom		Check is electric resistance is the same of point 20.5 or lower
26	**PHOTOLITHOGRAPHY-Mask 6_Cantilevers+Inlets**					

26.1	HDMS	Z1/Yes III HMDS	30' @ 125°C			DO HDMS! Otherwise no PR adhesion on SiN.
26.2	AZ ECI coating EBR PR Bake	Z1/Rite_track or ACS	C_AZ_ECI_5um or ACS program 0329 (HMDS included)	5 um		CD= 5 um (markers). Need EBR! Check the coating of polysilicon islands. I am concerned because I am using a 5um thick PR to coat a 6um thick step.
26.3	PR exposure	Z6/MA6 (or MLA)	xxx s, Soft Contact (or MLA: 220mJ/cm^2, -3, high quality)		MLA, 230mJ/cm^2	Alignment. Marker 3-6
26.4	PR development PR PostBake	Z1/Rite_track or ACS	Dev_AZ_ECI_5um or ACS program 0929			
26.5	Inspection	Z6/uScope	Resolution and alignment			
27	**LOW STRESS SILICON NITRIDE DRY ETCHING**					
27.1	Silicon Nitride Dry Etch	Z2/ A601E	Nitrure_1: ER=300nm/min, less than 5' (check final nitride thickness from wafer history)	depends on wafer, check		$ER_{\_PR}$=300nm/min. PR remaining after 5'=3.5 um. $ER_{\_ls\text{-}SiNx}$=280-300nm/min.
27.2	Inspection	Z6/uScope	Resolution and alignment			
28	**POLYSILICON DRY ETCHING**					
28.1	PolySilicon Dry Etch	Z2/ A601E	ANISO_ADP: 1'31"	6 um		$ER_{\_PR}$=130nm/min. PR remaining=3.3 um. $ER_{\_PolySi}$=4.5 um/min
28.2	Inspection	Z6/uScope	Resolution and alignment			
28.3	Etching check	Z3/Nanospec	Check Si+ls-SiN thickness	500 nm		
29	**LOW STRESS SILICON NITRIDE DRY ETCHING**					
29.1	Silicon Nitride Dry Etch	Z2/ A601E	Nitrure_1: 2'	500 nm		$ER_{\_PR}$=300nm/min. PR remaining=2.7 um. $ER_{\_ls\text{-}SiNx}$=280-300nm/min.
29.2	Inspection	Z6/uScope	Resolution and alignment			
29.3	Etching check	Z3/Nanospec	Check Si+ls-SiN thickness	0 nm		
30	**SILICON ETCHING**					
30.1	Bosch process	Z2/ A601E	ANISO_ADP: 2'30''	10 um		This will make release faster. (I should still have more than 2um PR). PR remaining=2.3 um. $ER_{\_Si}$=5 um/min.

30.2	SF6 Isotropic dry etching	Z2/ A601E	Si_release: 5'	30um width (15 um per side)		$ER_{\_PR}$=50nm/min. PR remaining=about 2 um um. $ER_{\_Si\ (lateral)}$=about 6um/min.
30.3	Inspection	Z6/uScope	Resolution and alignment			
30.4	SEM inspection	Z1/LEO	Check release, underetch release, stress, cantilever profiles			
30.5	Conductivity check	Z16/PM8	Check isolation between bottom and top contacts (R>MΩ). Check also isolation between different bottoms.	R=about 10 ohm on the same pad. R=Mohm betwenn dfferent tracks, and top/bottom		Check is electric resistance is the same of point 20.5 or lower
31	**CLEAVAGE**					
31.1	Cleaving in chips		Z1/back (cleavage table)	Try to follow cleavage lines.		Try to follow cleavage lines. Be as gentle as possible. Try to define a small line as deep and as vertical as possible, it has to reach the wafer edge. If when pushing down to break the wafer, it bends, DO NOT INSIST, but keep scratching the line.
31.2	Inspection	Z6/uScope	Resolution and alignment			

Drawings


Tolérances générales ISO 2768-f
Toutes les faces polies
ECHELLE 2:1
SECTION A-A
SECTION B-B
PMMA
Connector v4.0 (4)
A3



SECTION A-A

Tolérances générales ISO 2768-m

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:	FINISH:	DEBURR AND BREAK SHARP EDGES	DO NOT SCALE DRAWING	REVISION	
	NAME	SIGNATURE	DATE	TITLE:	
DRAWN					
CHK'D					
APPV'D					
MFG					
Q.A					
MATERIAL: Acier inoxydable				DWG NO. KF25 adapter	A4
WEIGHT:				SCALE:2:1	SHEET 1 OF 1